

68HC11 CPU Board for 170 Controllers

Extending the life of the 170e Controller



By selecting the 68HC11 processor we have modernized the 170e. The 68HC11F1 MPU as the new processor, is widely used in the electronics industry and is available from at least 3 manufacturers.

Below is a list of benefits and advantages of 170 HC11 CPU Board:

1. Extending the life of a well-established product and continuing to serve our customer base that has standardized on the 170.
2. The new CPU speed has been increased from 1.53MHZ to 2.45MHZ allowing better handling of communication and other tasks.
3. Processor speed can be doubled in the future if necessary.
4. PROM memory is increased by 32K bytes allowing more complex programs. (A 32 pin ZIF socket shall be used for PROM memory.)
5. Greater memory expansion possible in the future.
6. Existing 170E's may be easily upgraded by the installation of a new 68HC11 CPU. This will allow users to take advantage of newly developed programs for the 68HC11 170 in installed controllers. The new CPU will plug into most Safetran and McCain Traffic Supply 170E controllers.
7. Interface to co-processor modules is provided for increased processing power.
8. BITran Systems and Wapiti will support the 170HC11 format.
9. Industry standard SPI serial bus is supported.

The reverse side is a copy of a specification for the Model 68HC11 CPU board.



68HC11 CPU Board for 170 Controllers

1. The purpose of this specification is to define a replacement CPU board for the existing 6800 based CPU board in the standard 170E controller.
2. The 68HC-11 based CPU Module shall operate a 68HC11F1 MPU to replace the existing 6800 MPU installed in the existing 170E CPU board. The MPU shall operate with the crystal frequency of 9.8MHz. The MPU chip shall be the socket mounted in an AMP PLCC socket #821547-1 series HPT or equal.
3. The 6850 communication IC's shall be used and shall operate with a crystal frequency of 9.8MHz. There shall be (4) chips (6850) with the programmable jumpers to select 5 different communication baud rates per chip (1200, 2400, 4800, 9600, 19,200, and 38,400) for a total of 25 jumpers. There shall be no IRQ inhibits provided therefore all ACIA's shall be active. Programs should be written to initialize the four communications chips upon startup. An IRQ status register shall be provided as defined in the 170E Caltrans spec.
4. The EPROM and RAM shall be resident on the CPU board, and shall be socket mounted. The EPROM socket shall be a 32-pin ZIF force Device. The RAM socket shall be a 28 pin Augat 828 series or equal.
5. RAM will be continuous from locations \$0000 to \$6FFF. RAM shall be a ZERO power device exclusively, and be a Dallas 1230 or equal. The RAM shall be a Dallas 1744 or equal. (Clock address shall be in the I/O map at location \$7FF8 to \$7FFF.)
6. A jumper select shall be provided to switch locations \$6000 to \$6FFF from Internal to External for access to the remote Dual Port location. The status of the jumper position shall be read on the IRQ register-bit five (5). When an enhanced Program Module is used with this system, it will only have access to addresses \$6000/6FFF for dual port.
7. The PROM chip shall be either a 32K x 8 or a 128K x 8 device, and be jumper selectable.
8. When using a 128K EPROM, a bank switch shall be enabled within the EPROM memory system. This bank switch shall function by moving to the upper 64K segment of the EPROM. The bank switch jumper controls address line A16. The bank shall be activated by a write to location \$7002 (directly connected to Port G on 68HC11 MPU), which will cause memory to go to the upper 64K of the 128K EPROM. This will enable an extra 32K of EPROM memory via bank switching. The status of A16 will read on the IRQ status register-bit six (6).
9. Feature and location switches shall be provided on the front portion of the CPU board. Each switch shall be an 8-position front reading dip switch. These switches shall be decoded as follows: Features switch shall be addressed at \$700A - Port E. Location Switches shall be addressed at \$7000 - Port A.
10. A header shall be provided near the front of the module for the SPI and serial interface pins.
11. There shall be one LED indicator located on the front of the CPU board, that shall be controlled via a software output of Port G bit 3.
12. The +12VDC, +5VDC and -12VDC voltages Input in the CPU board shall have transorb protection.
13. The system address organization of the 68HC11 Module shall consist of nine addressing configurations.
14. The nine addressing configurations shall be selectable by use of three-post jumpers. The following input line state conditions shall cause the Decoder to provide the associated address configuration. The jumper shall be labeled "INT" and "EXT," MAPI and MAP2.
15. Each CPU board shall be furnished with a blank EPROM chip.
16. The CPU board shall fit in both the McCain and Safetran 170E controllers.