2070E LA CITY

Controller

USER MANUAL

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1 2070E LA CITY CONTROLLER

1.1 PRODUCT DESCRIPTION

The 2070E LA City Controller is a ruggedized, multitasking field processor and communications system that is easily configurable for a variety of traffic management applications in either a rack or shelf mount configuration.

The 2070E LA City Controller has a general purpose nature, open architecture and modular design, and its functionality depends on the software loaded into the controller and the modules included.

McCain's 2070E LA City Controller, is designed in full compliance with Caltrans Transportation Electrical Equipment Specifications (TEES) 2009 and Errata 1 Jan 21st 2010.

The McCain's 2070E LA City Controller's primary function is intersection control but can be used for a multitude of applications based on the controller's software.

The controller's OS/9 operating system provides a robust, flexible and expandable platform that is compatible with multi-vendor application control software.

1.2 BENEFITS

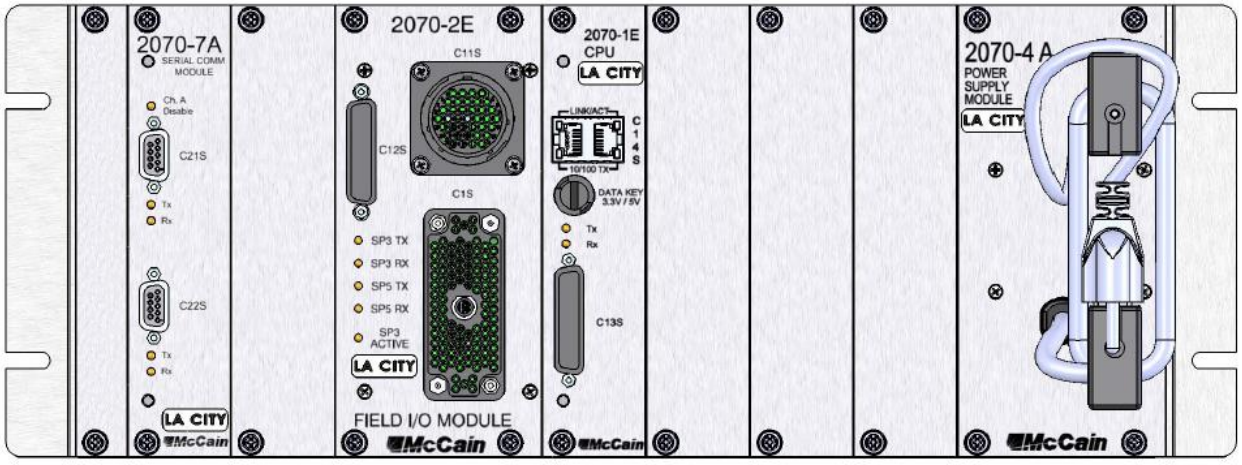
- Open Architecture insures compatibility with off-the-shelf products OS/9 Software – Standard Software Modules from Multiple Sources.
- Flexible Design to Meet Specific User Needs.
- The controller's multitasking operating system (OS) supports a variety of applications.
- Easily upgrades current intersection hardware.
- Multitasking – Each 2070E LA City Unit Can Control Multiple Applications.
- Physically Compatible with Model 170&170E Controllers & Facilities.

1.3 CONFIGURATION

This controller configuration is constructed as follows (See Figure 1):

- 2070E Chassis unit
- 2070-1E LA City CPU module
- 2070-2E LA City Field I/O module
- 2070-3A LA City Front Panel module
- 2070-4A LA City Power Supply module
- 2070-7A LA City Asynchronous Serial Communications module
- Blank filler plates: There are four 2X and one 1X

FRONT VIEW



REAR VIEW

Figure 1: 2070E LA City Controller, Front and Rear Views

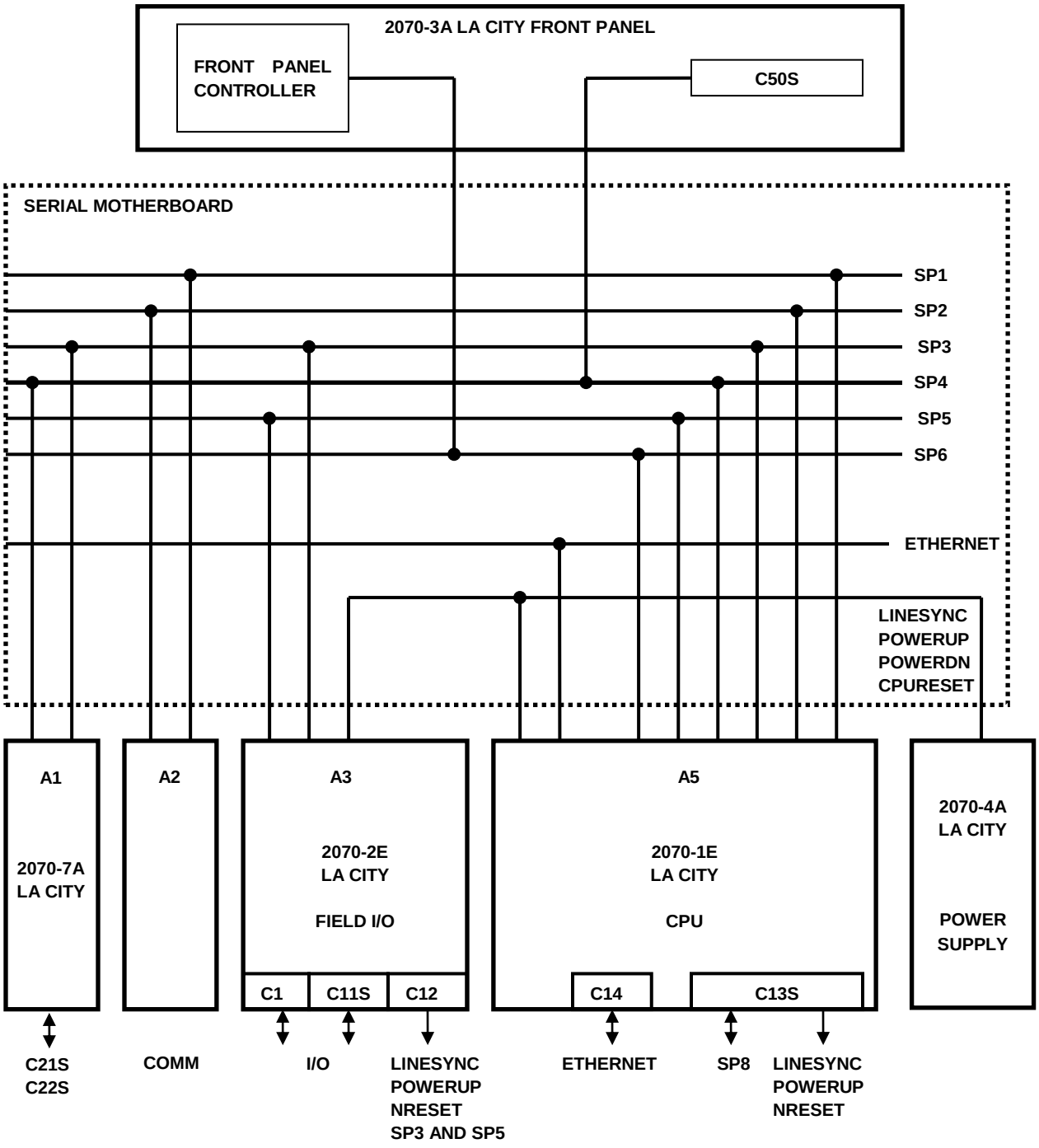


Figure 2: 2070E LA City Controller System Configuration

1.4 STANDARD FEATURES

Operating system

- Microware Embedded OS-9

Modules (standard, included)

- 2070-1E LA City CPU Module
- 2070-2E LA City Field I/O module
- 2070-3A LA City Front Panel Module
- 2070-4A LA City Power Supply
- 2070-7A LA City Asynchronous Serial Communications module.

Microprocessors

- CPU Module: Freescale MC68EN360, 32 Bit, 24.576 MHz microprocessor
- I/O Module: Freescale MC68LC302 microprocessor, running at 20 MHz

Backup real-time clock (RTC)

- Texas Instrumens BQ4845S-A4N

Memory

- 32 MB PSRAM (Main RAM).
- 8 MB Flash Memory.
- 2 MB NonVolatile-SRAM.

Applicable standards

- Meets or exceeds Caltrans TEES 2009 standard with additional considerations specific to the City of Los Angeles' specifications.

1.5 INTERFACES

Communication interfaces

- 2 SDLC, 5 ACIA (up to 38Kbps).
- Ethernet (10 Mbps I802-3(TP) 10 BASE-T Standard) wired to an integrated 10/100Mbps Ethernet Switch.

Front panel interface

- Display: 4 lines x 40 characters
- Keyboards: 3 x 4 navigation and 4 x 4 data entry keypads

Cabinet interfaces

- C11S Connector
- C12S Connector
- C1S Connector

2 2070-1E LA CITY CPU MODULE

2.1 GENERAL DESCRIPTION

The 2070-1E LA City CPU Module is the brain of the controller. It includes the microprocessor computer chip, memory, serial communications and operating system. The 2070-1E LA City is a module meeting the 2X WIDE board requirements. The module is furnished normally resident in the Slot A5 of Motherboard.

The 2070-1E LA City Assembly consists of a Printed Circuit Board Assembly and a front plate. The front plate is attached to the board by using two screws and two washers.

The 2070-1E LA City microprocessor is a Freescale MC68EN360 running at 24.576 MHz.

It consists of a Host Board, an Engine Board and a faceplate (plus brackets, standoffs and hardware to fix them to the host board).

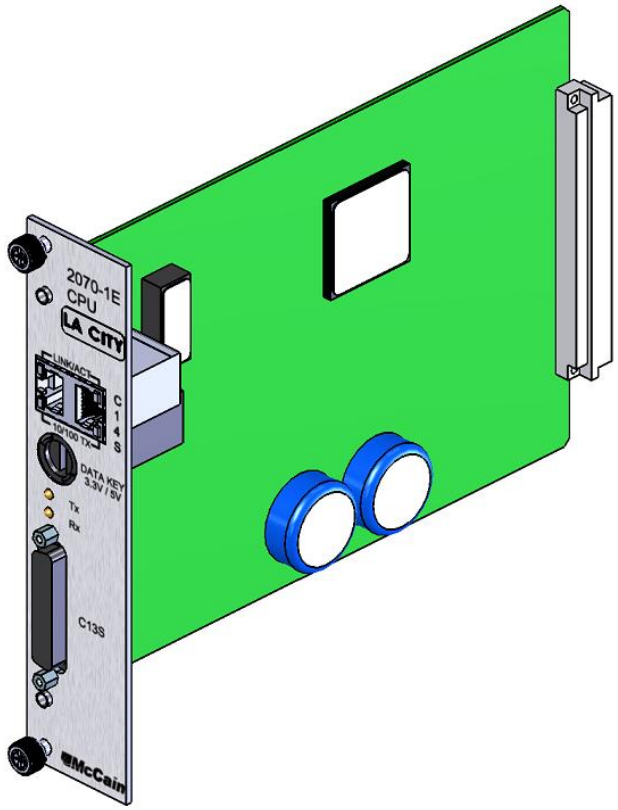


Figure 3: 2070-1E LA City CPU Module

2.2 STANDARD FEATURES

- Processor: Freescale MC68EN360, 32 Bit, 24.576 Mhz, CPU32 Instruction Set.
- Memory
  - 256Mbit (8 M x 32 Bits) PSRAM (Main RAM)
  - 64Mbit (4 M x 16 Bits) Flash Memory
  - 16Mbit (1 M x 16 Bits) NonVolatile-SRAM
- Comm
  - 2 SDLC, 5 ACIA (up to 38Kbps)
  - Ethernet (10 Mbps I802-3(TP) 10 BASE-T Standard) wired to an integrated 10/100Mbps Ethernet Switch
- Serial Buses: EIA RS-485 to Motherboard (6 COMM + modem control).
- Time-of-day clock
- Security: DATAKEY provides multiple levels of human access
- Interrupts
- CPU reset
- CPU activity LED
- Tick timer

2.3 COMMUNICATION INTERFACES' DESCRIPTION

Serial Port 1 (SP-1):

Usage: This is a general purpose port.

Location: available at the DIN-96 connector.

Operating modes: Asynchronous, Synchronous, HDLC, SDLC.

Async rates (bps): 1200, 2400, 4800, 9600, 19.2k, 38.4k / Optional: 57.6k, 115.2k.

Sync rates (bps): 19.2k, 38.4k, 57.6k, 76.8k, 153.6k.

Interface pins:

SP1_TXD: Transmit Data (O)

SP1_RXD: Receive Data (I)

SP1_RTS: Request To Send (O)

SP1_CTS: Clear To Send (I)

SP1_CD: Carrier Detect (I)

SP1_TXC_INT: Transmit Clock Internal (O)

SP1_TXC_EXT: Transmit Clock External (I)

SP1_RXC_EXT: Receive Clock External (I)

Serial Port 2 (SP-2):

Usage: This is a general purpose port.

Location: available at the DIN-96 connector.

Operating modes: Asynchronous, Synchronous, HDLC, SDLC.

Async rates (bps): 1200, 2400, 4800, 9600, 19.2k, 38.4k / Optional: 57.6k, 115.2k.

Sync rates (bps): 19.2k, 38.4k, 57.6k, 76.8k, 153.6k.

Interface pins: SP2_TXD: Transmit Data (O)

SP2_RXD: Receive Data (I)

SP2_RTS: Request To Send (O)

SP2_CTS: Clear To Send (I)

SP2_CD: Carrier Detect (I)

SP2_TXC_INT: Transmit Clock Internal (O)

SP2_TXC_EXT: Transmit Clock External (I)

SP2_RXC_EXT: Receive Clock External (I)

Serial Port 3 (SP-3):

Usage: To handle in-cabinet devices.

Location: available at the DIN-96 connector.

Operating modes: Asynchronous, Synchronous, HDLC, SDLC.

Async rates (bps): 1200, 2400, 4800, 9600, 19.2k, 38.4k / Optional: 57.6k, 115.2k.

Sync rates (bps): 153.6k, 115.2k.

Interface pins: SP3_TXD: Transmit Data (O)

SP3_RXD: Receive Data (I)

SP3_RTS: Request To Send (O)

SP3_CTS: Clear To Send (I)

SP3_CD: Carrier Detect (I)

SP3_TXC_INT: Transmit Clock Internal (O)

SP3_TXC_EXT: Transmit Clock External (I)

SP3_RXC_EXT: Receive Clock External (I)

Serial Port 4 (SP-4):

Usage: External user interface and general purpose.

Location: available at the DIN-96 connector.

Operating modes: Asynchronous.

Async rates (bps): 1200, 2400, 4800, 9600, 19.2k, 38.4k / Optional: 57.6k, 115.2k

Interface pins:

SP4_TXD: Transmit Data (O)

SP4_RXD: Receive Data (I)

Serial Port 5 (SP-5):

Usage: To handle in-cabinet devices.

Location: available at the DIN-96 connector.

Operating modes: Synchronous, HDLC, SDLC.

Sync rates (bps): 153.6k, 614.4k.

Interface pins:

SP5_TXD: Transmit Data (O)

SP5_RXD: Receive Data (I)

SP5_TXC_INT: Transmit Clock Internal (O)

SP5_RXC_EXT: Receive Clock External (I)

Serial Port 6 (SP-6):

Usage: Front panel user interface.

Location: available at the DIN-96 connector.

Operating modes: Asynchronous.

Async rates (bps): 1200, 2400, 4800, 9600, 19.2k, 38.4k / Optional: 57.6k, 115.2k

Interface pins:

SP6_TXD: Transmit Data (O)

SP6_RXD: Receive Data (I)

Serial Port 8 (SP-8):

Usage: General purpose.

Location: available at the C13S connector on Front plate.

Operating modes: Asynchronous, Synchronous, HDLC, SDLC.

Async rates (bps): 1200, 2400, 4800, 9600, 19.2k, 38.4k / Optional: 57.6k, 115.2k.

Sync rates (bps): 19.2k, 38.4k, 57.6k, 76.8k,153.6k.

Interface pins:

SP8_TXD: Transmit Data (O)

SP8_RXD: Receive Data (I)

SP8_RTS: Request To Send (O)

SP8_CTS: Clear To Send (I)

SP8_CD: Carrier Detect (I)

SP8_TXC_INT: Transmit Clock Internal (O)

SPI (Serial Peripheral Interface):

Usage: Ethernet communication and DATAKEY.

Location: DataKey's receptacle at Front plate and serial EEPROM on Host Board.

Operating modes: Synchronous.

Sync rates (bps): Application specific.

Interface pins:

SPI_MOSI: Master-Out-Slave-In (O)

SPI_MISO: Master-In-Slave-Out (I)

SPI_CLK: Clock (O)

SPI_SEL_1: Select 1 (O)

SPI_SEL_2: Select 2 (O)

SPI_SEL_3: Select 3 (O)

SPI_SEL_4: Select 4 (O)

Ethernet Interface (ENET):

Usage: Local and Network Communications.

Location: Two 10/100BASE-T Ethernet ports on Front plate.

Operating modes: Synchronous, Manchester-encoded, Differential.

Sync rates (bps): 10M, 100M.

The Ethernet switch uses the ports as follow:

ENET1P0 to communicate to the Ethernet transceiver (IC2).
ENET1P1 and ENET1P2 to communicate signals to/from the C14S connector.
ENET1P3 available at the P2 header.
ENET1P4 to communicate signals to/from the A5 connector at the Backplane.

2.4 THEORY OF OPERATION

The 2070-1E LA City CPU consists of a single PCB assembly and a metal panel fixed by two screws and two washers.

The assembly contains all of the control circuitry for the CPU functions: main processor, FLASH memory, SRAM, PSRAM, RTC, a bidirectional buffer bank for the data, address lines and control lines coming from the processor, a slave processor, the back-up capacitors, RESET circuit, isolation circuit for control signals coming from the power supply, isolation circuit for SP8, C13S connector, C14S connector, Ethernet circuit, DATAKEY circuit, driver filed circuit (RS 485 transceivers), LINESYNC circuit, A2 and A3 connector sensor, and A5 connector.

Main Processor

The 2070-1E LA City CPU uses the MC68360 Quad Integrated Communication Controller as the main processor, it is clocked by and external 24.576MHz oscillator. The term "quad" comes from the fact that there are four serial communications controllers (SCCs) on the device. However, there are actually seven serial channels which include four SCCs, two serial management controllers (SMCs), and one serial peripheral interface (SPI).

This processor handles the system buses, memory, serial communication ports (SP2, SP3, SP4, SP5 and SP6), Ethernet communication and DATAKEY through SPI port; it also generates the CPU RESET and FPA LED signals.

Slave Processor

This a MC68LC302 clocked by an external 16MHz oscillator. This processor handles the serial communication ports SP1, SP8 and the baud rate for SP4.

Clocks

These different clock signals are used on the CPU.

24.576MHz oscillator is used for the main processor MC68EN360.

16MHz oscillator is used for the slave processor MC68LC302.

20MHz oscillator is used for the Ethernet interface transceiver.

25MHz oscillator is used for the Ethernet switch.

32.768KHz crystal is used for the RTC circuit.

Address Bus

This is a bidirectional 23-bit bus (A0-A22) capable of addressing up to 4GByte of data.

Data Bus

This is a bidirectional 32-bit bus (D0-D31) used to carry data among the processors, memories and other system devices.

Decoding Signals

The signals for write enable, /OE, R/W', CHIP SELECTS are used themselves and also are combined into a glue logic stage in order to generate the required signals for the control and interaction among the devices.

Buffer Circuit

This circuit consists of four octal bus transceivers SN74LVC245 and five octal bus transceivers SN74LVC541 used to translate signals as data, address and some control lines from and to the other board devices.

Transceivers SN74LVC245 connect the 32-lines data bus (D0-D31) from processor to other board devices (memories, slave processor, RTC) and vice versa. The transceivers are enabled by the input /G that is connected to the line D CSDB; when this line is HIGH the buses are effectively isolated, when LOW the buses are enabled. The direction of the bus is controlled by the input DIR that is connected to the line /DOE; when this line is LOW, communication is from bus B to bus A, when HIGH it is from bus A to bus B.

Transceivers SN74LVC541 connect the 23-lines address bus from processor to other board devices (memories, slave processor, RTC) and vice versa. The transceivers are enabled by the inputs /OE1 and /OE2 that are tied to GND, then the buses are always enabled.

A5 connector

This 96-pin DIN connector is the physical interface between CPU and serial motherboard. It carries the RS 485 differential signals for the communication ports S1 to SP6, the interruption signals LINESYNC, POWERUP and POWERDN, the Ethernet transmission and reception lines, the +5VDC, +5VSTD and +12VISO, A2 and A3 install lines, and the CPURESET and FPALED lines.

C13S Connector

This is a DB25 connector containing the RS 485 differential line communication signals for the SP8, the external control signals from 2070 power supply also as RS 485 signals and the +5VDCISO power.

A2 and A3 Connector Sensor

This circuit is used to let know the CPU when the A2 and/or A3 slots on serial motherboard are being used.

It is made of two inverter gates SN74LV04 (U18A and U18B) with pull-up and connected to the sensing lines on A5 connector, these two lines come from the A2 and A3 slot connectors on serial motherboard. The output of the inverter gates is LOW until A2 and/or A3 are used.

A2INSTALL: When A2 slot on serial motherboard is used, this line goes to GND forcing the output of U18A to HIGH. This line enables the differential line drivers for SP1 and SP2 transmission.

A3INSTALL: When A3 slot on serial motherboard is used, this line goes to GND forcing the output of U18B to HIGH. This line enables the differential line drivers for SP5 transmission.

Linesync Circuit

It is used to generate the /IRQ5 for processor, this interruption occurs on both rise and fall flanges of LINESYNC signal.

It is implemented with two D-Type Flip-Flop SN74LV74, one inverter gate SN74LV04 and two buffer gates 74LV125.

The two clear outputs are tied to +5VDC.
The two data input are tied to GND.

LINESYNC signal coming from 2070 power supply module is fed to CLK2, it is also inverted and fed to CLK1.

The buffer gates' inputs are tied to GND.

When LINESYNC transitions from LOW to HIGH at CLK2, Q2 goes to LOW and enables U19D generating a LOW output.

When LINESYNC transitions from HIGH to LOW, inverter gate convert it to a LOW to HIGH transition at CLK1, Q1 goes to LOW and enables U19C generating a LOW output.

The two active LOW preset inputs are connected to a pull-up and to the LINESYNC_CTL line; that is, the outputs Q1 and Q2 of U6 are set to HIGH by using this line every time the processor receives the /IRQ5.

CPU Reset Circuit

This circuit receives the reset from main processor through the CPU LRESET line and sends the reset to A5 connector through the CPURESET line; this reset is used by the other modules connected to serial motherboard.

It is formed by using an inverter gate, two resistors, and one NPN transistor.

The logic status received from CPU is inverted two times, one by the inverter gate and another one for the transistor; that is, CPURESET has the same logic status as CPU LRESET.

The output of the inverter gate is also connected to the optocoupler OP6 input 2 (input 1 is POWERUP inverted), the outputs of this optocoupler are tied and connected to a differential line driver (DV2 channel 2) to generate NRESET differential signals for C13S connector.

FPA LED Circuit

The main processor activates/deactivates Q1's base through CPULED line; then FPA line goes to A5 connector, this signal is used by the front panel assembly (FPA) to activate/deactivate ACTIVE LED.

Memory

FLASH

There are 8MB of FLASH memory configured as 4M X 16bit on the FLASHMEM1, 6MB are available for AGENCY use and 2MB are used to store the boot image that is the software program that controls processor operation.

It is accessed by using zero wait states and chip select /(L CS0) at /CE, enabled at /WE and /OE through the lines /(L R/W') and /(L OE) respectively.

For performing a read operation /CE must be LOW, and /OE must be LOW.

For a write operation/CE must be LOW and /WE must be low.

SRAM 1M X 16bit

This 16M memory (SRAM3), 1M X 16bit, is used to store all of the non-volatile data, it has a battery back-up in order to avoid losing data during a power failure on AC line. This memory is accessed using zero wait states and chip select /(CS-RAM) at /CE1.

For performing a read operation /CE1 must be LOW and /OE must be LOW.

For a write operation, /CE1 must be LOW and R/W' must be LOW, also /LB and /UB must be selected in order to define what byte is being written.

PSRAM 2M X 32bit

This is a bank containing two Pseudo-Static RAM, they are configured as 8M X 32bit are used as the main RAM.

It is addressed by 23 address lines (A2 to A24), accessed using zero wait states and chip select /(L RAS1) at /CE1.

PSRAM1 stores data corresponding to D0 to D15

PSRAM2 stores data corresponding to D16 to D31.

Read operation for both memories is /CE1 must be LOW, /OE must be LOW and /WE must be HIGH.

Write operation for both memories is /CE1 must be LOW, /WE must be LOW and /OE must be HIGH. The selection for what byte is going to be written is done through the enable inputs /LB and /UB of each memory, this enable inputs are controlled by the lines /(LM-WE) and /(LU-WE) for PSRAM1, and /(UM-WE) and /(UU-WE) for PSRAM2.

RTC

Implemented by a parallel real-time clock with CPU supervisor and external SRAM non-volatile memory backup BQ4845S-A4N and a 32.768KHz external quartz crystal.

It is addressed by the address lines A0 to A3, allowing access to the 16 bytes of real-time clock and control registers. The RTC is connected to the data bus at D24 to D31 in order to provide 8bit of real-time clock information.

It is controlled by the lines:

/CS chip select input, connected to the line /CS5.
/CE IN Chip enable Input, connected to the line /CS4.
/CE OUT Chip enable Output, connected to the line /CSrtcSRAM.
/OE Output enable, provide the read control for the RTC memory locations.

DATAKEY

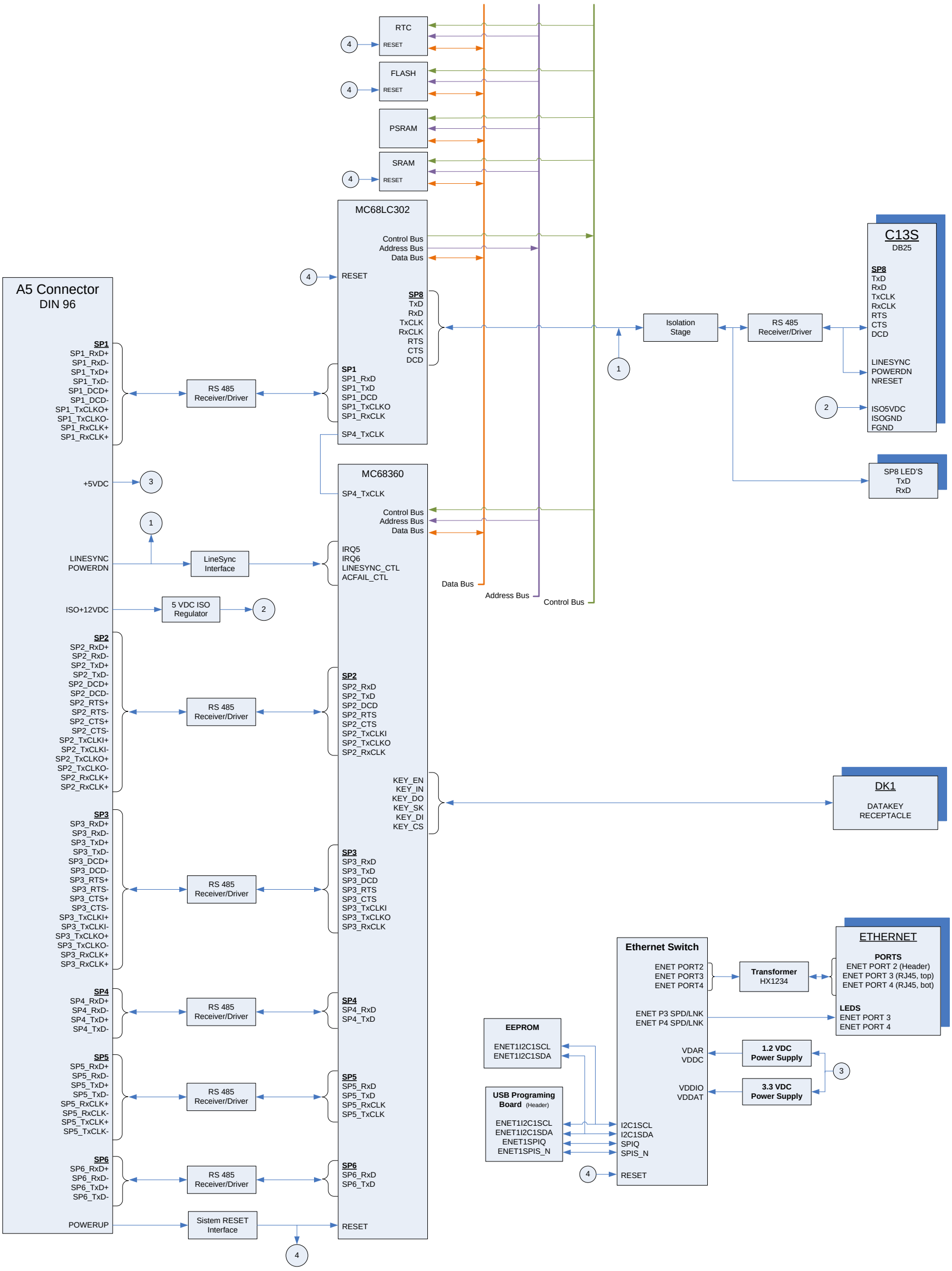
This circuit consists of a serial memory key receptacle which contains a Last-On/First-OF (LOFO) switch that ensures the key do a secure contact before any signal is transmitted and support circuitry for interfacing it with the processor.

It is implemented by using a DATAKEY receptacle KC4210PCB, three buffer gates SN74LV125 and one PNP transistor BC807.

For any Data Key operation the OS9 data key driver samples the LOFO line, if the line is cleared (logic LOW 0V) then the driver powers up the data key to begin the requested operation. After the operation is finished the data key is powered down until another operation is requested.

Once the data key has been detected and energized by the LOFO switch, the driver tries to communicate using the I2C protocol to get the drive ID and memory size, if there is no response, it tries again with the SPI protocol if this also results in a no response situation then all communication with the data key is halted until a new operation is requested (an error code will be generated when this event occurs). After a response is successfully obtained from the data key the requested operation will begin, if any error is detected during the operation an error code will be returned and communications will be halted.

2.5 2070-1E LA CITY BOARD BLOCK DIAGRAMS



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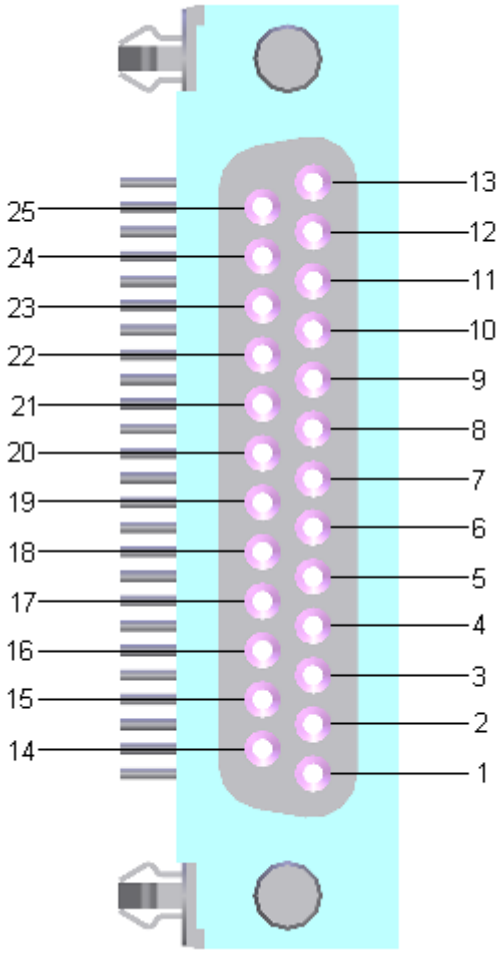
2.6 CONNECTORS' PIN OUT:

C13S Connector (DB25 Female):

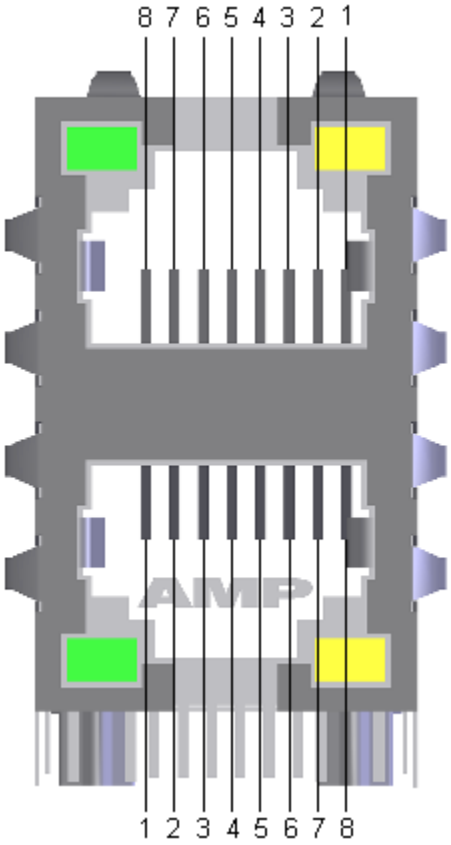
Pin	Function
1	SP8_TxD+
2	SP8_RxD+
3	SP8_TxCLK+
4	SP8_RxCLK+
5	SP8_RTS+
6	SP8_CTS+
7	SP8_DCD+
8	n/a
9	LINESYNC+
10	NRESET+
11	POWERDN+
12	ISO+5VDC
13	ISOGND
14	SP8_TxD-
15	SP8_RxD-
16	SP8_TxCLK-
17	SP8_RxCLK-
18	SP8_RTS-
19	SP8_CTS-
20	SP8_DCD-
21	n/a
22	LINESYNC-
23	NRESET-
24	POWERDN-
25	FGND



Ethernet Connector, ETH 1/2 (RJ45):

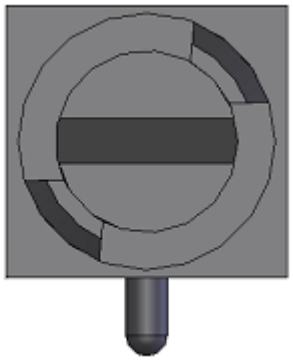
ENET 1 Port 3 (Up)	
Pin	Function
1	Tx+
2	Tx-
3	Rx+
4	Unused
5	Unused
6	Rx-
7	Unused
8	Unused

ENET 1 Port 4 (Down)	
Pin	Function
1	Tx+
2	Tx-
3	Rx+
4	Unused
5	Unused
6	Rx-
7	Unused
8	Unused



Datakey receptacle connector:

Pin	Function
1	nc
2	Ground
3	VCC
4	nc
5	Data out
6	Chip select
7	Serial clock
8	Data in
9	Data in
10	Serial clock
11	Chip select
12	Data out
13	nc
14	VCC
15	Ground
16	nc
17	LOFO
18	LOFO



2.7 2070-1E LA CITY MODULE DIMENSIONS

The 2070-1E LA City CPU Module has the following dimensions:

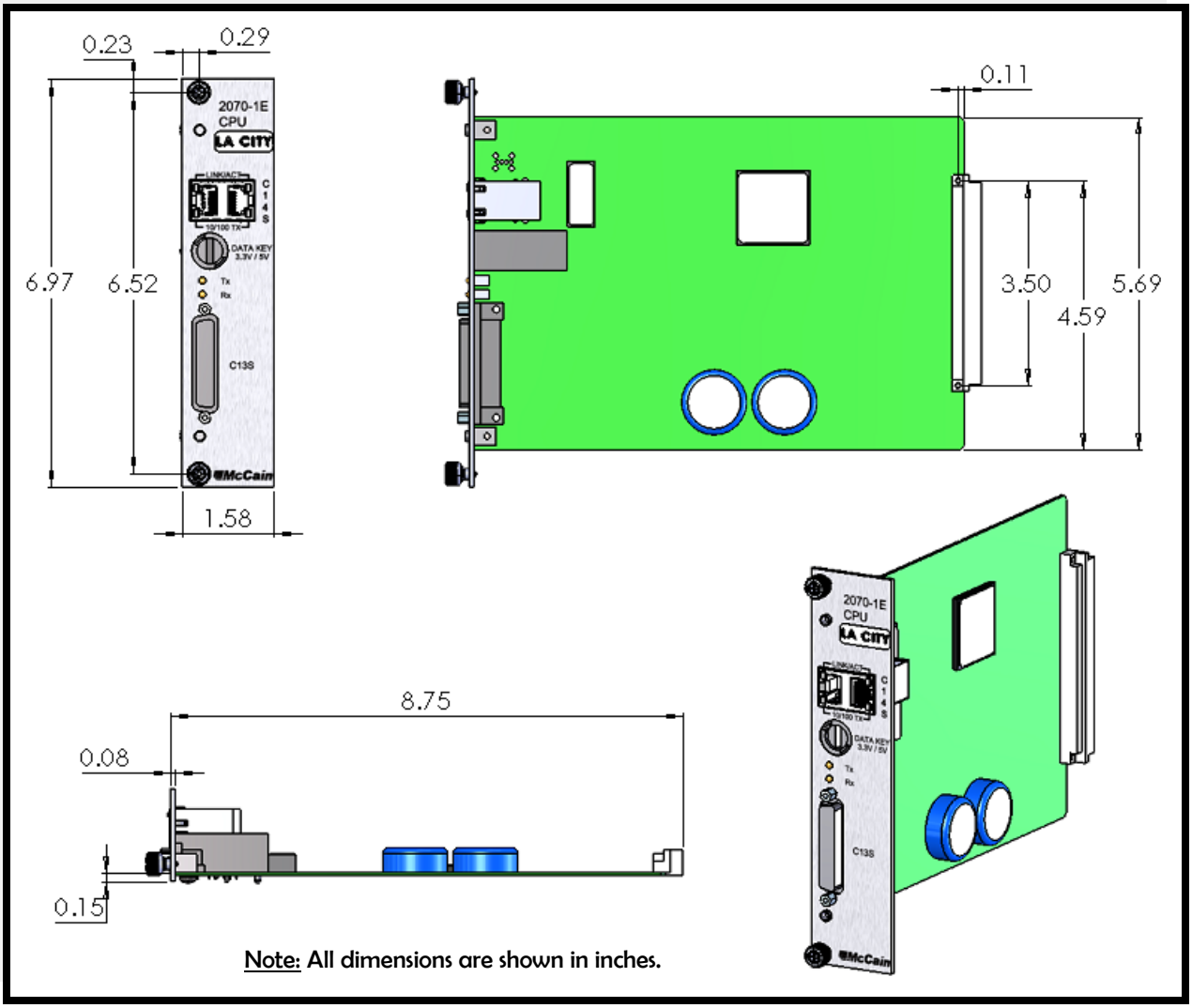


Figure 4: 2070-1E LA City CPU Dimensions

2.8 ADJUSTMENT

The 2070-1E LA City CPU module has no adjustments to be applied.

2.9 INSTALLING THE 2070-1E LA CITY CPU MODULE

Follow these steps to complete the 2070-1E LA City CPU module installation into the Controller.

Turn off the controller using the power switch located in the front plate of 2070-4A LA City Module.

Slide the 2070-1E LA City CPU into slot A5 thru the card guides. Press the module into the backplane and tighten the thumbscrews until the CPU module is secure.

3 2070-2E LA CITY MODULE, FIELD I/O MODULE

3.1 GENERAL DESCRIPTION

The 2070-2E LA City Field I/O Module fully meets with the TEES 2009; it serves as an interface between the controller and the external world through its parallel I/O interface and two serial ports present at the front connectors.

The Field I/O module provides a parallel interface with 64 inputs/outputs present at C1S and C11S; also, a serial interface is provided through the SP-3 and SP-5 serial ports present at C12S connector, transmission and reception status indicators for both ports and a “SP-3 ACTIVE” port indicator are located at the front plate.

The Field I/O module is optically isolated from the rest of the 2070E LA City Controller.

The 2070-2E LA City Field I/O Module consists of:

- C1S and C11S Connectors: Provides 64 inputs and 64 outputs for control of equipment.
- C12S Connector: Provides the SP-3 and SP-5 serial ports, the control signals LINESYNC, NRESET and POWERDOWN, and +5VDC ISO.
- A 2070 Type main board: Contains all necessary circuitry for implementing the 2070-2E LA City functions.
- A 4X face plate: Provides mechanical support and identification in the Controller.

Figure 5: 2070-2E LA City Module

3.2 THEORY OF OPERATION.

The Field I/O module provides the interface between the controller and the external world, so that it contains all hardware and software needed for performing its functions as established into the TEES 2009.

The module contains a processor, SRAM, FLASH, parallel input/output ports, muzzle jumper, serial communication circuitry, C1S, C11S and C12S connectors installed on the front panel plate; serial communication circuitry, power Supply (+12VDC and +5VDC); and required software.

Processor

It is a Freescale MC68LC302 Integrated Multiprotocol Processor; it has a static 68008 core and a flexible communications architecture. The processor is running at 20MHz generated by an external oscillator.

Memory

SRAM

The 4Mbit Static RAM is used to execute code, store and retrieve all variable and temporary data.

It uses an 18-bit address bus (A0 to A17) and a 16-bit data bus (I/O 0 to I/O 15).

There is a glue logic stage to decode the signals from the control bus and handle the SRAM; this stage receives the signals and generates the proper signals for enabling the SRAM, for selecting the read/write operations and for selecting the low byte or upper byte.

FLASH

A 4Mbit FLASH memory is used in order to store the firmware. It is a non-volatile memory and serves as a media for storing program code and nonvolatile data so that if power is removed the stored data is not lost.

It uses an 18-bit address bus (A0 to A17) and a 16-bit data bus (I/O 0 to I/O 15).

Control signals

The control signals POWERUP, POWERDOWN and LINESYNC are signals coming from the Power Supply and are generated according to the conditions of the AC input power; CPURESET is a signal coming from the CPU and it is a software reset. They are received through the A3 slot; all are inverted and isolated before using them as follow:

POWERUP and CPURESET:

- These signals are OR'ed at the isolation stage, resulting into the NRESET signal.
- It enables a buffer gate to generate a reset signal that goes to the microprocessor and FLASH memory.
- It is converted to EIA-485 differential signals and routed to the C12S connector.

LINESYNC:

- Once the LINESYNC is isolated it is inverted again, then the inverted and not-inverted signals go to the processor.
- It is converted to EIA-485 differential signals and routed to the C12S connector.

POWERDOWN:

- It is converted to EIA-485 differential signals and routed to the C12S connector.

SP-3 and SP-5 Serial ports

SP-5

The module receives the SP-5 transmission signals (TxD and TxC) through the A3 connector; they are converted from EIA-485 signals to single ended signal, inverted and converted to multidrop isolated ports, then one is routed to the processor and the other one is converted to EIA-485 signals again then routed to the C12S connector mounted on the front plate.

The SP-5 reception signals (RxD and RxC) come from the C12S connector; they are converted from EIA-485 signals to single ended signal, opto-isolated, converted to differential signals and then routed to the A3 connector.

Field SP-5 enable signal (FSP5_EN): This signal disables the EIA485 line driver for the SP-5 reception signals (RxD and RxC) that come from the C12S connector and at the same time it enables the SP-5 reception signals (RxD and RxC) from the processor's communication port in order to send them to the A3 connector.

SP-3

The module receives the SP-3 transmission signals (TxD and TxC) through the A3 connector; they are converted from EIA-485 signals to single ended signal, inverted, isolated, converted to EIA-485 signals again then routed to the C12S front connector.

The SP-3 reception signals (RxD and RxC) come from the C12S connector; they are converted from EIA-485 signals to single ended signal, opto-isolated, converted to differential signals and then routed to the A3 connector.

- SP-3 enable switch (S1):

  The "S1" toggle switch located on the main board connect/disconnect the transmission and reception of the SP-3 serial port in the Field I/O module in order to prevent a multiple use.

  The switch enables/disables the EIA-485 line driver and receiver that handle this serial port by forcing the enable input to ground.

  Switch at "ON" position, SP-3 is available at C12S connector, "SP3 ACTIVE" LED is turned on.

  Switch at "OFF" position, SP-3 is NOT available at C12S connector, "SP-3 ACTIVE" LED is turned off.

LED's status indicators

The status indicator circuits for transmission and reception consist of an inverter gate, an LED and a current limiting resistor in series.

- The "SP3 Tx" and "SP5 Tx" LED status indicator circuits are driven by the corresponding single ended transmission signal already isolated.

- The "SP3 Rx" and "SP5 Rx" LED status indicator circuit are driven by the corresponding single ended reception signal coming from the EIA-485 receiver at the isolated side.

- The "SP3 ACTIVE" status indicator circuit consists in a current limiting resistor and an LED; it is driven by the "S1" toggle switch. Indicator is turned on when switch is at "ON" position and turned off when the switch is at the "OFF" position.

- The "ACTIVE" LED status indicator circuit for the SP-5 consists of an LED and current limiting resistor in series; this circuit is driven directly by the microcontroller.

    - The Fast Flash (10Hz) condition means that the SP-5 communication is present.

    - The Slow Flash (1Hz) condition means that the SP-5 communication is not present.

    - If there is a steady condition either "ON" or "OFF" then there is a fault condition.

RESET

Processor has two input pins called /HALT and /RESET which are tied handled by the line /RESETH, when this line is in LOW state then processor is said to be RESET. There are four sources for generating the /RESETH line, the watchdog circuit, the supervisory circuit, the NRESET circuit and the BDM circuit.

Watchdog

A watchdog circuit is used to force a system reset and protect against system failures when the program is not executed as expected. This circuit provides a means to escape from unexpected input conditions, external events, or programming errors. The watchdog counter is cleared by the program periodically so that it never reaches its timeout value, otherwise a system failure occurred and then a system reset is applied to force the system back to a known starting point.

The circuit is implemented by using a D-Type flip—flop that receives two inputs from the processor (watchdog control and the watchdog reset lines), its output (watchdog flag) goes to the watchdog input at processor.

The watchdog control input presets the output to LOW state; watchdog reset serves as a clock input transferring the input to the output, forcing the output to HIGH state because the input is tied to ground. Watchdog flag keeps the watchdog status and it is monitored by the processor after the reset condition in order to know if it was because a watchdog "no service" condition as a result of a program malfunction.

WDT enable shunt:
A watchdog timer enable shunt is provided on the module. It consists of a 3-positions header (JP1) and a jumper to be placed at either ON or OFF position.

- Jumper at ON position (pin-1 to pin-2): The processor outputs a state change on OUTPUT 39 (Monitor Watchdog Timer Input) every 100ms for 10 seconds or due to Set Output Command. The watchdog output is sent to the output port #5 bit 8 and located at C1S connector pin-103.

- Jumper at OFF position (pin-2 to pin-3): Causes no watchdog output. This feature is required to operate with the Model 210 Monitor Unit.

Supervisory circuit

The supervisory circuit monitors the power supply of the processor and it asserts a reset if the power supply drops below the threshold level of 4.63 VDC. The reset is an active low output that remains low by 140ms once power supply reaches the threshold level.

NRESET

This signal is the result of OR'ing the POWERUP and CPURESET signals at the isolation stage.

POWERUP is a signal from the Power Supply and is generated according to the conditions of the AC input power; it is asserted if a power failure lasts more that 525ms ±25ms.

CPURESET is a signal coming from the CPU and it is a software reset.

They are received through the A3 slot, inverted, OR'ed and isolated. The NRESET signal enables a buffer gate to generate the /RESETH signal that asserts the reset pin at processor.

BDM port

There is a 10-positions connector header (BDM) on the main board and it is used as a manufacturer-specific BDM interface port for in-circuit programming and test on-board devices.

Parallel I/O ports

The parallel I/O ports consist of 64 input and 64 outputs that are present at the front connectors C1S and C11S, see CONNECTOR's PIN OUT section to see physical correspondence.

The front connectors are located on the connector board which is plugged to the main board through a 150-positions receptacle connector, so that the 64 inputs and 64 outputs reach the main board and are routed to their corresponding circuits.

Parallel inputs ports

64 inputs using ground-true logic are provided; each input has an internal 10KOhm pull-up resistor to the ISO +12VDC and a resistive network in order to adequate the signal so that the input is a logic "1" when the input voltage at its field connector input is less than 3.5VDC, and is logic "0" when the input voltage exceeds 8.5VDC.

The 64 inputs are distributed on eight octal buffers / line drivers; in order to send these inputs to the processor they are arranged into four 16-bit groups called input banks.

Each input bank is formed of two octal buffers, receives 16 inputs from the resistive network and sends the corresponding 16-bits of information to the CPU through the data bus when its corresponding enable input is asserted.

Bank 1 (formed by port 1 and port 2) handle the inputs 1 to 16.

Bank 2 (formed by port 3 and port 4) handle the inputs 17 to 32.

Bank 3 (formed by port 5 and port 6) handle the inputs 33 to 48.

Bank 4 (formed by port 7 and port 8) handle the inputs 49 to 64.

This lines for enabling and disabling the four input banks come from a 3-line to 8-line decoder. The decoder accepts the lines A1, A2 and A3 from the address bus to select a bank, two active-low enable inputs for the chip select and output enable and one active-high enable input for the line that clear the output banks.

The parallel input ports' stage is powered with ISO +5VDC.

Parallel outputs ports

64 outputs using ground-true logic are provided; outputs written as a logic "1" have sink-current capability and outputs written as a logic "0" provide an open circuit. Each output is capable of driving 50 VDC and sinking 150mA.

The 64 outputs are distributed on eight octal D-Type latches; in order to send these outputs to the field connectors they are arranged into four 16-bit groups called output banks.

Each output bank is formed of two octal D-Type latches, receives 16-bits of information from the CPU through the data bus and sends the corresponding 16 outputs to the field connectors at the positive edge of the clock input.

Bank 1 (formed by port 1 and port 2) handle the outputs 1 to 16.

Bank 2 (formed by port 3 and port 4) handle the outputs 17 to 32.

Bank 3 (formed by port 5 and port 6) handle the outputs 33 to 48.

Bank 4 (formed by port 7 and port 8) handle the outputs 49 to 64.

This lines for enabling and disabling the four output banks come from a 3-line to 8-line decoder. The decoder accepts the lines A1, A2 and A3 from the address bus to select a bank, two active-low enable inputs for the chip select and output enable and one active-high enable input for the line that clear the output banks.

The line for enabling/disabling the output banks is connected to the clock input pin of the corresponding octal D-Type latch, when this input goes to high, information at the inputs are transferred to the outputs on the positive going edge of the clock pulse. When the clock input is at either the high or low level, the input signals have no effect at the outputs.

The parallel output ports' stage is powered with ISO +5VDC.

Connectors

150-Positions header
This is a 150-pins high density 2mm male header connector used to interconnect the main board (which support all of the input/output, power, isolation and control circuitry) and the connector board (which support all of the necessary connectors for the field interface) that has the mating female receptacle.

A3 Connector
It is a 96-pin right angle DIN connector used to interface the Field I/O module to the serial mother board.

It carries the signals and power lines for:

- The serial ports SP-3 and SP-5.
- The control signals: LINESYNC, POWERUP, POWERDOWN and CPURESET.
- The +5VDC voltage that is used to feed the circuitry at the non-isolated side, the line driver and line receiver, the inverter gates, the opto-isolators and the toggle switch.
- The +12VDC ISO voltage that is then converted to +5VDC ISO in order to feed all Control and I/O circuitry.

Isolation Stage

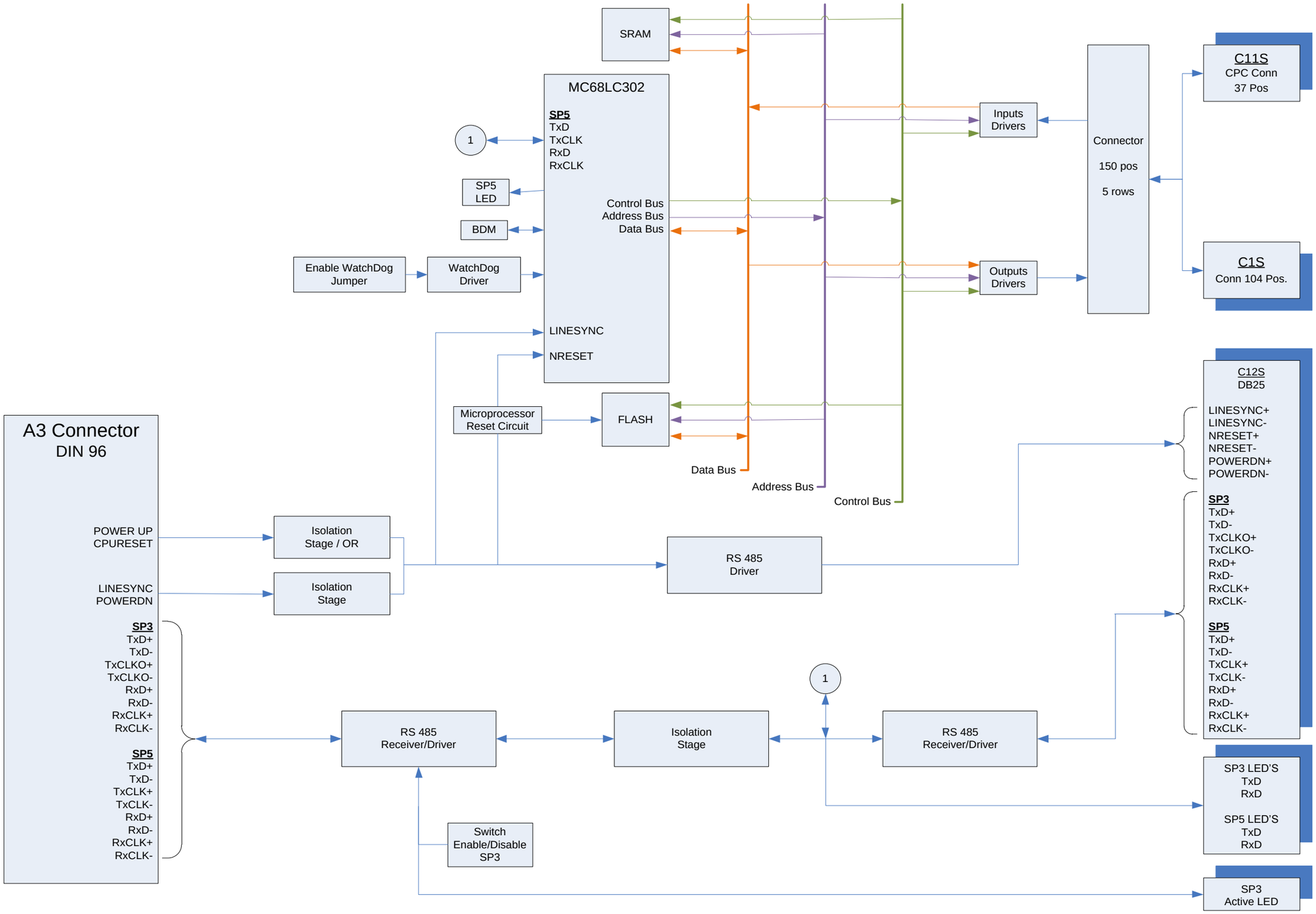
The Field I/O module is the module for interfacing the Controller with the real world so that it is isolated from the system in order to avoid all kind of problems related to the field such as ground loops, induced noise, etc.

The module optically isolates the transmission and reception lines of serial ports SP-3 and SP-5; therefore, all communication lines between the CPU and Field I/O module are isolated.

The serial ports come from the CPU through the Serial Motherboard and are present at A3 connector; the RS485 communication signals entering to the Field I/O module are converted to single ended lines and are then isolated; also, the communication lines going to the CPU are isolated and then converted to RS485 signals. The isolation is achieved by using optically coupled logic gates that combine a light emitting diode and a photo detector. The detector's output is an open collector transistor. This stage provides circuit isolation and high speed logic interfacing at induced noise environments.

The Control and I/O circuitry is fed with +5VDC ISO, that is obtained from the ISO +12VDC coming from the 2070-4A LA City Power Supply and present at A3 connector.

3.3 2070-2E LA CITY BLOCK DIAGRAM



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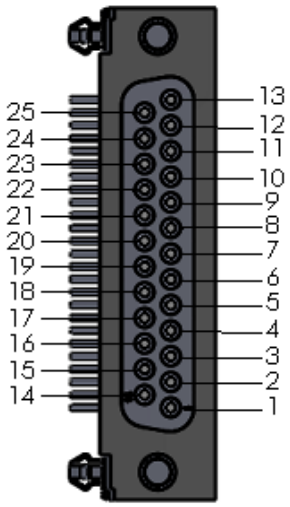
3.4 CONNECTORS' PIN OUT

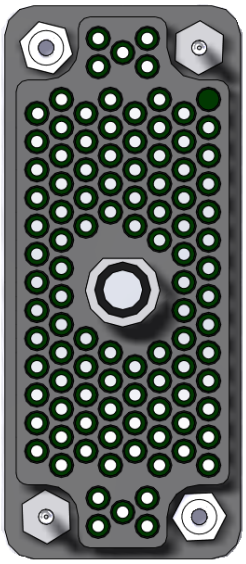
Connector C12S (DB25 Female):

Pin	Function	Pin	Function	Pin	Function
1	SP5 TxD+	11	POWERDN+	21	SP3 RxCLK-
2	SP5 RxD+	12	ISO VCC	22	LINESYNC-
3	SP5 TxCLK+	13	ISO GND	23	NRESET-
4	SP5 RxCLK+	14	SP5 TxD-	24	POWERDW-
5	SP3 TxD+	15	SP5 RxD-	25	FGND
6	SP3 RxD+	16	SP5 TxCLK-		
7	SP3 TxCLKO+	17	SP5 RxCLK-		
8	SP3 RxCLK+	18	SP3 TxD-		
9	LINESYNC+	19	SP3 RxD-		
10	NRESET+	20	SP3 TxCLKO-		



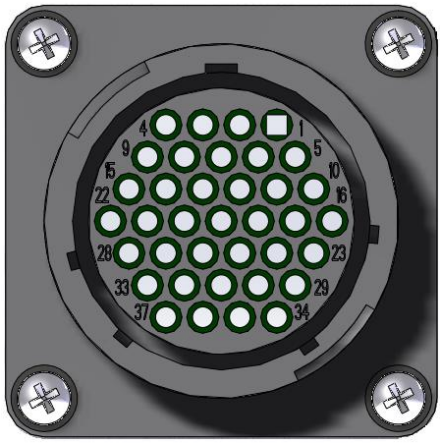
Connector C1S:

Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	DCG #2	27	O24	53	I14	79	I44
2	O0	28	O25	54	I15	80	I45
3	O1	29	O26	55	I16	81	I46
4	O2	30	O27	56	I17	82	I47
5	O3	31	O28	57	I18	83	O40
6	O4	32	O29	58	I19	84	O41
7	O5	33	O30	59	I20	85	O42
8	O6	34	O31	60	I21	86	O43
9	O7	35	O32	61	I22	87	O44
10	O8	36	O33	62	I23	88	O45
11	O9	37	O34	63	I28	89	O46
12	O10	38	O35	64	I29	90	O47
13	O11	39	I0	65	I30	91	O48
14	DCG #2	40	I1	66	I31	92	DCG #2
15	O12	41	I2	67	I32	93	O49
16	O13	42	I3	68	I33	94	O50
17	O14	43	I4	69	I34	95	O51
18	O15	44	I5	70	I35	96	O52
19	O16	45	I6	71	I36	97	O53
20	O17	46	I7	72	I37	98	O54
21	O18	47	I8	73	I38	99	O55
22	O19	48	I9	74	I39	100	O36
23	O20	49	I10	75	I40	101	O37
24	O21	50	I11	76	I41	102	O38 DET RES
25	O22	51	I12	77	I42	103	O39 WDT
26	O23	52	I13	78	I43	104	DCG #2



Connector C11S:

Pin	Function	Pin	Function
1	O56	20	I53
2	O57	21	I54
3	O58	22	I55
4	O59	23	I56
5	O60	24	I57
6	O61	25	I58
7	O62	26	I59
8	O63	27	I60
9	DCG #2	28	I61
10	I24	29	I62
11	I25	30	I63
12	I26	31	DCG #2
13	I27	32	NA
14	DCG #2	33	NA
15	I48	34	NA
16	I49	35	NA
17	I50	36	NA
18	I51	37	DCG #2
19	I52		



3.5 2070-2E LA CITY MODULE DIMENSIONS

The 2070-2E LA City Field I/O has the following dimensions

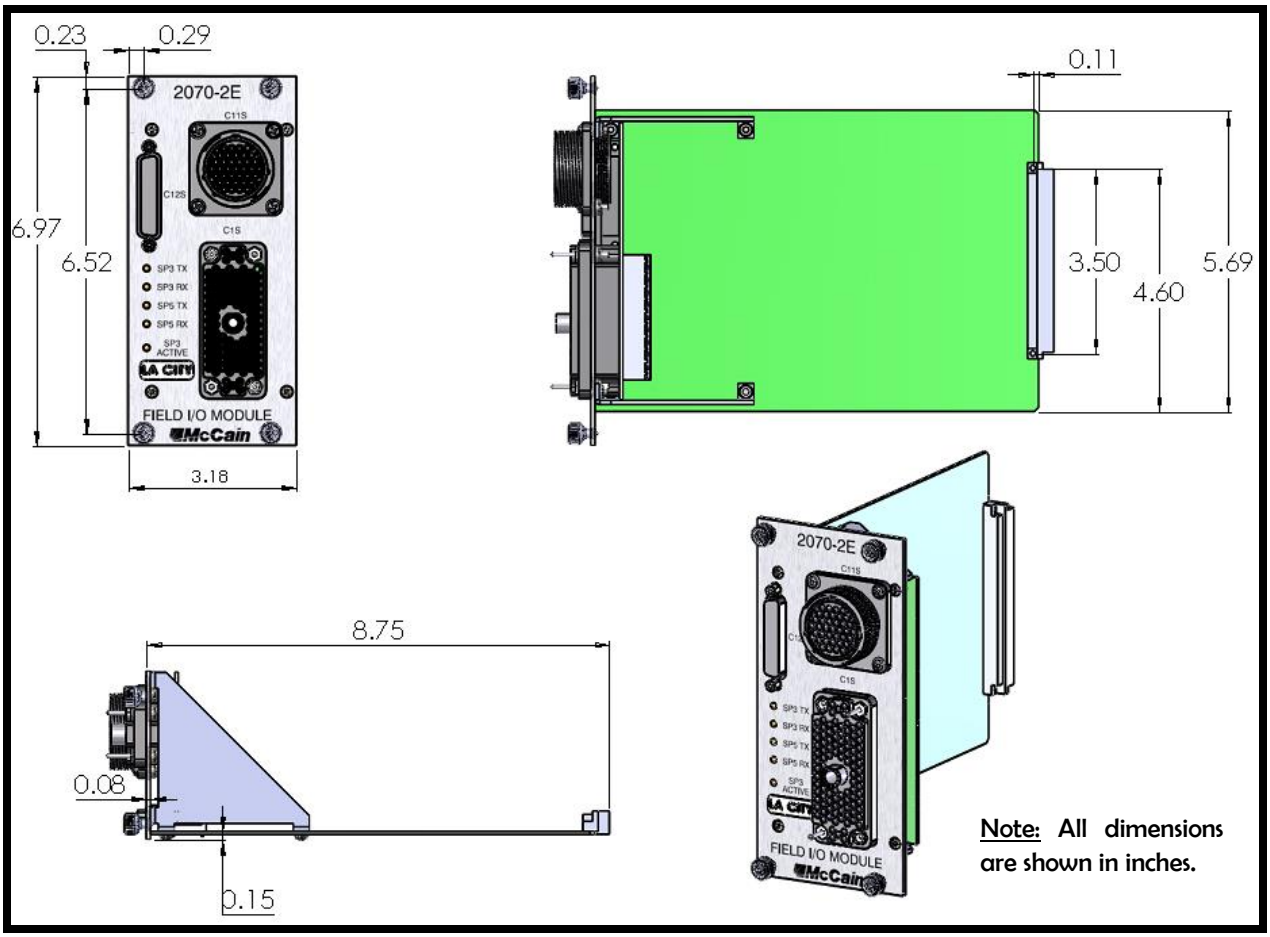


Figure 6: 2070-2E LA City Dimensions

3.6 INSTALLING THE 2070-2E LA CITY MODULE

Normally the module is attached to the controller, but this section contains information of installation of the 2070-2E LA City in case it is not.

1. Turning off the controller using the power switch located in the front plate of 2070-4A LA City Module.
2. Slide the 2070-2E LA City into slot A3 thru the car guides. Press the module into the backplane; tighten the thumbscrews until the module is secure.

These steps complete the 2070-2E LA City installation into the 2070E LA City Controller.

4 2070-7A LA CITY MODULE, ASYNC COMMUNICATION SERIAL BOARD

4.1 GENERAL DESCRIPTION

The 2070-7A LA City Module is a hot swappable asynchronous serial communication module that extends and isolates the Controller's serial communication ports available on the serial motherboard slots A1/A2 to the Controller's rear panel for field connections.

The module provides two 9-positions D-sub female connectors on the face plate, C21S as channel 1 and C22S as channel 2. The opto-isolated communication channels have LED indicators for Tx and Rx status.

The serial ports handled are the SP-1/SP-2 if the module is installed into the A2 slot and the SP-3/SP-4 if installed into the A1 slot.

Both channels can be manually disabled; when Channel 1 is disabled, Channel "A" LED is turned on. Channel 2 can be disabled by the "C50 enable" signal present at "A1" connector Pin-B21.

The 2070-7A LA City Asynchronous Module consists of:

- C21S Connector: Provides the SP-1 or SP-3 to the field.
- C22S Connector: Provides the SP-2 or SP-4 to the field.
- LED status indicators: For Tx and Rx on both C21S and C22S; for Channel "A" disable.
- A 2070 Type board: Contains all necessary circuitry for implementing the 2070-7A LA City functions.
- A 2X face plate: Provides mechanical support, necessary cutouts and identification.

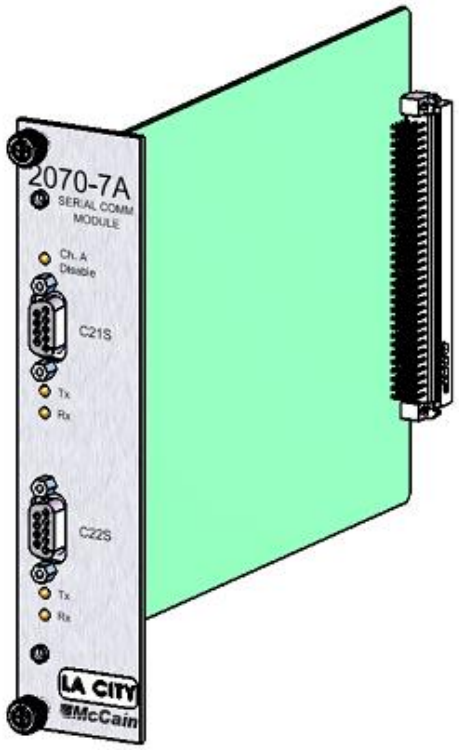


Figure 7: 2070-7A LA City Module

4.2 THEORY OF OPERATION

The 2070-7A LA City Module provides two independent asynchronous serial communication channels that are opto-isolated in order to handle field signals without affecting the Controller. Both channels can be manually disabled and one channel can be disabled by the C50 enable line.

Asynchronous serial communications

The RS-485 transmission signals (Tx and RTS) coming from the serial motherboard enter to the module through the A1/A2 slot; then they are converted from differential signals to single ended signal, opto-isolated, converted to RS-232 differential signals and then routed to the C21S and C22S connectors located on the front face of the module.

The RS-232 reception signals (Rx, CTS and DCD) coming from the C21S and C22S connectors located on the front of the module are converted from differential signals to single ended signal, opto-isolated, converted to RS-485 differential signals and then routed to the serial motherboard.

LED status indicator circuit

The circuit consists of an inverter gate, a LED and a current limiting resistor in series.

The Tx LED status indicator circuit is driven by the single ended Tx signal coming from the opto-isolator. The Rx LED status indicator is driven by the single ended Rx signal coming from the RS-232 device output.

Enabling/disabling circuits

Both Channel 1 and 2 can be manually disabled by using a jumper; the enable line is normally connected to a pull-up resistor, the jumper forces the line to logic ground disabling the differential line drivers. When disabled the Channel “A” LED indicator is turned on.

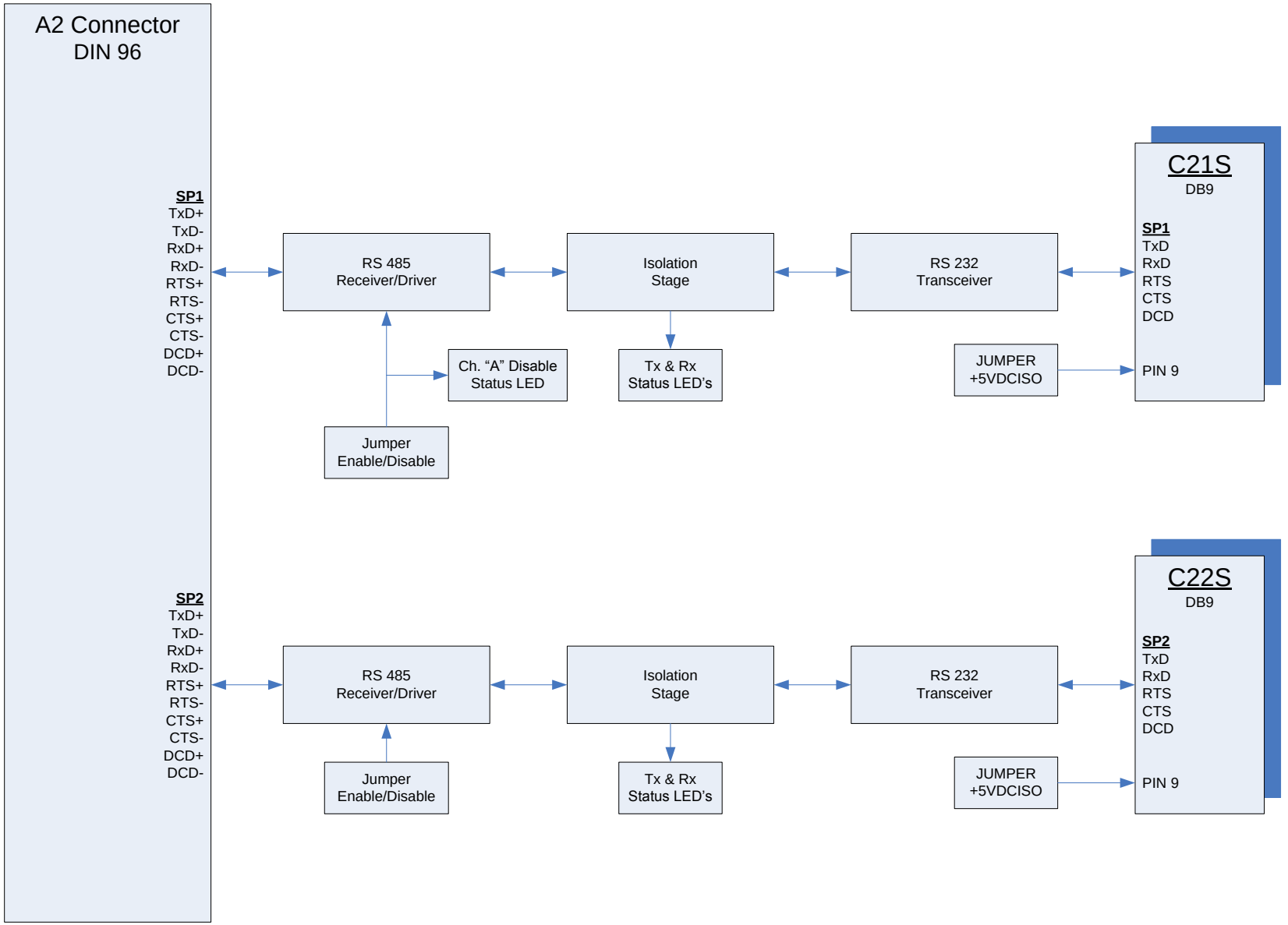
Channel 2 can be disabled by the “C50 enable” signal present at “A1” connector Pin-B21; the enable line is normally connected to a pull-up resistor, the “C50 enable” line coming from the A1/A2 connector forces the line to logic ground disabling the differential line drivers.

Isolated power supply

The isolated power supply is obtained by using a DC/DC converter; this device is fed by the +12VDC ISO line, the output is a +5VDC isolated power supply for all the related circuitry for C21S and C22S.

By using a jumper, the +5VDC isolated power supply can be individually connected to the Pin-9 of the C21S and/or C22S connector.

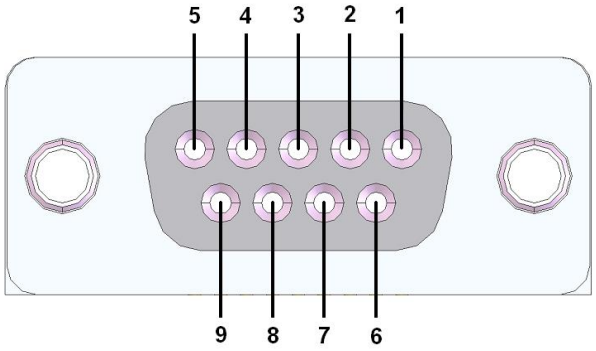
4.3 2070-7A LA CITY BLOCK DIAGRAM



4.4 CONNECTORS' PIN OUT:

Connector C21S (DB9 Female):

Pin	Function
1	SP1 DCD
2	SP1 RXD
3	SP1 TXD
4	nc
5	IFC GND
6	nc
7	SP1 RTS
8	SP1 CTS
9	+5VDC ISO



Connector C22S (DB9 Female):

Pin	Function
1	SP2 DCD
2	SP2 RXD
3	SP2 TXD
4	nc
5	IFC GND
6	nc
7	SP2 RTS
8	SP2 CTS
9	+5VDC ISO

4.5 THE 2070-7A LA CITY MODULE DIMENSIONS

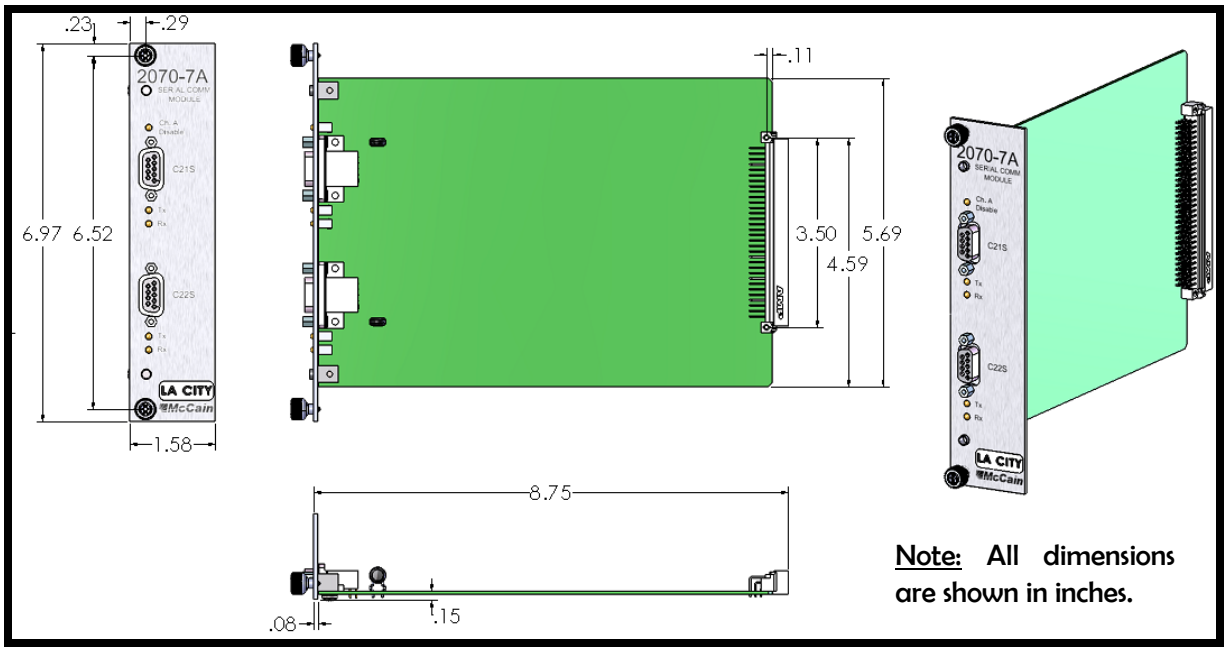


Figure 8: 2070-7A LA City Dimensions

4.6 ADJUSTMENT

The 2070-7A LA City provides two headers for independently enabling/disabling the communications channels.

Placing a jumper at “J1” header, the channel 1 (SP-1/SP-3) at C21S is disabled (See figure 9).

Placing a jumper at “J2” header, the channel 2 (SP-2/SP-4) at C22S is disabled (See figure 9).

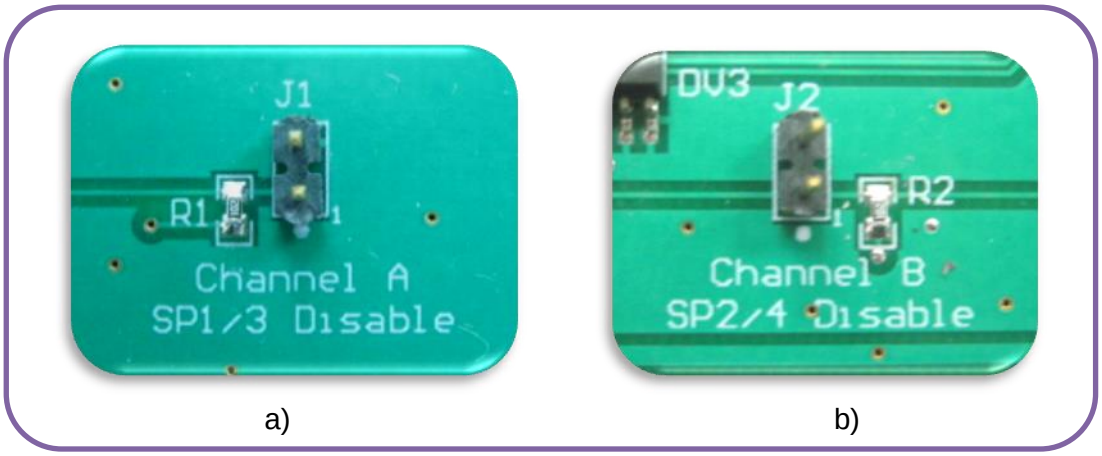


Figure 9: Jumpers J1 and J2

The 2070-7A LA City provides two headers for connecting/disconnecting the +5VDC isolated power supply from the front connectors:

Placing a jumper at “J3” header, the pin-9 at C21S is powered with an isolated +5VDC (See figure 10).

Placing a jumper at “J4” header, the pin-9 at C22S is powered with an isolated +5VDC (See figure 10).

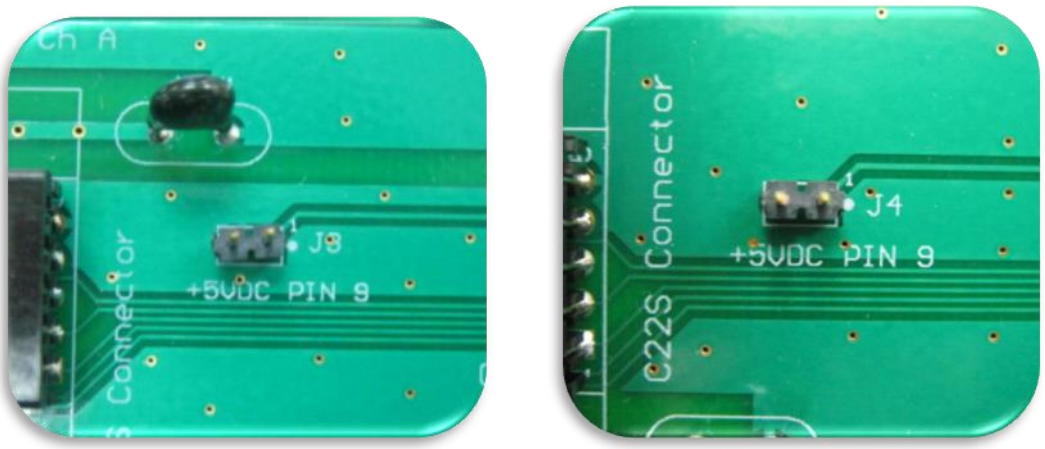


Figure 10: Jumpers J3 and J4

4.7 INSTALLING THE 2070-7A LA CITY MODULE

Normally the module is attached to the Controller, but this section contains information of installation of the 2070-7A LA City in case it is not.

1. Turn off the controller using the power switch located in the front plate of 2070-4A LA City Power Supply.
2. Verify that the module has the jumpers installed in accordance with the expected functionality.
3. Slide the 2070-7A LA City into slot A2 thru the card guides. Press the module into the backplane; tighten the thumbscrews until the module is secured.

These steps complete the 2070-7A LA City Module installation into the Controller.

The 2070-7A LA City Module is a hot swappable module because it can be installed and removed while the controller is working without damage to the circuitry.

5 2070-3A LA CITY MODULE, FRONT PANEL ASSEMBLY

5.1 GENERAL DESCRIPTION

The Front Panel Assembly (FPA) provides a user interface via keypads and the LCD display, also the module has the serial port SP-4 available through the C50S connector for a terminal's connection. Also an ACTIVE LED to show the application's status, an AUX switch and a LCD's contrast knob are available; the Front Panel assembly also serves as a swinging door to cover the back of the Chassis and the Serial motherboard when closed.

The assembly consists of:

- An 4 line by 40 character display and a LCD's contrast knob.
- Keyboard interfaces: a 4x4 alphanumeric keyboard and a 3x4 cursor and symbol keyboard.
- C50S connector: Provides a connection to the SP-4.
- An AUX switch.
- An ACTIVE LED.
- A P2 connector: for interfacing the PCB assembly to the LCD display.
- A P3 connector: for interfacing the module to the CPU through the Serial motherboard.
- A RESET switch: for a manual reset of the Front panel assembly.
- A sliding latch and latch guide.
- Two thumbscrews for a mechanical attachment to the Chassis unit.
- A sub-assembly board: contains all necessary circuitry for implementing the FPA functions.
- A metal panel: provides mechanical support, necessary cutouts and identification.

The Figure 11 shows the 2070-3A LA City module.

Figure 11: 2070-3A LA City Module

5.2 THEORY OF OPERATION

Microcontroller

The FREESCALE M9S12E64 runs at 24.576MHZ and performs all necessary functions of the Front Panel assembly: communicates to the CPU via the serial asynchronous port SP-6, scans the keypads and displays messages on the LCD display, controls the LCD backlight, generates the BELL signal, monitors the AUX switch and the manual RESET switch.

Keyboards

The keyboard interface is comprised of a 4x4 keyboard (sixteen keys for hexadecimal alphanumeric entry) and a 3x4 keyboard (twelve keys for cursor control and symbol entry).
All of the lines connected to these two keyboards go directly to the M9S12E64 microcontroller.

P2 and P3 connectors

P2: This 16-positions connector is the interface from the FPA's PCB assembly to the LCD display. It carries the data and command lines from microcontroller to the LCD unit, the intensity control from the contrast knob and the backlighting control.

P3: This 40-positions connector is the interface to the Serial motherboard in order to connect the communications lines for the SP-6 port and SP-4 port and the control lines ACTIVE LED and RESET coming from the CPU.

C50S Connectors

The C50S is a 9-positions D-sub female connector. This connector provide the asynchronous serial port SP-4 from the CPU to be used as a terminal's connection and the C50 enable line that serves to sense if the C50S connector is being used or not, this prevents the SP-4 port be used at the same time on the front connector and at A1 connector on Serial motherboard.

SP-4 circuitry

The related circuitry consists of one RS-232 transceiver and two RS-485 transceivers that implement the interface for transmitting and receiving data to and from the SP-4 coming from the CPU.

The RS-485 transceiver receives the SP-4 transmission differential signals coming from the P3 connector and converts them to a single end signal; this signal enters to the RS-232 transceiver whose output is connected to the Tx pin at C50S connector.

The Rx pin at C50S connector receives the SP-4 reception signal and route it to the RS-232 transceiver whose output is connected to the RS-485 transceiver, then the differential signals are then routed to the P3 connector.

The C50 enable circuit

This line is normally forced to High state through a 10K pull-up resistor to Vcc; it is connected to the driver's input of a RS-485 transceiver whose differential outputs are connected to the enable pins of the RS-485 transceiver that handle the SP-4 communication; while the driver's input is high, the enable inputs disable the SP-4 communications and the C50 enable signal goes to high, this signal is one of the differential outputs and it is routed to P3 connector.

Bell

It is an electronic bell controlled by the microcontroller used to signal receipt of ^G (hex 07) and RESET condition. It is performed by a buzzer which is managed by the microcontroller applying a 2 KHz square signal for a period of 350mS.

AUX Switch

This is a toggle switch that forces the status of the STOPTIME line from microcontroller to Low by connecting a pull-up to logic ground. The microcontroller receives the status of this line and sends a code to the CPU through the P3 connector; this information is used according to the application running in CPU.

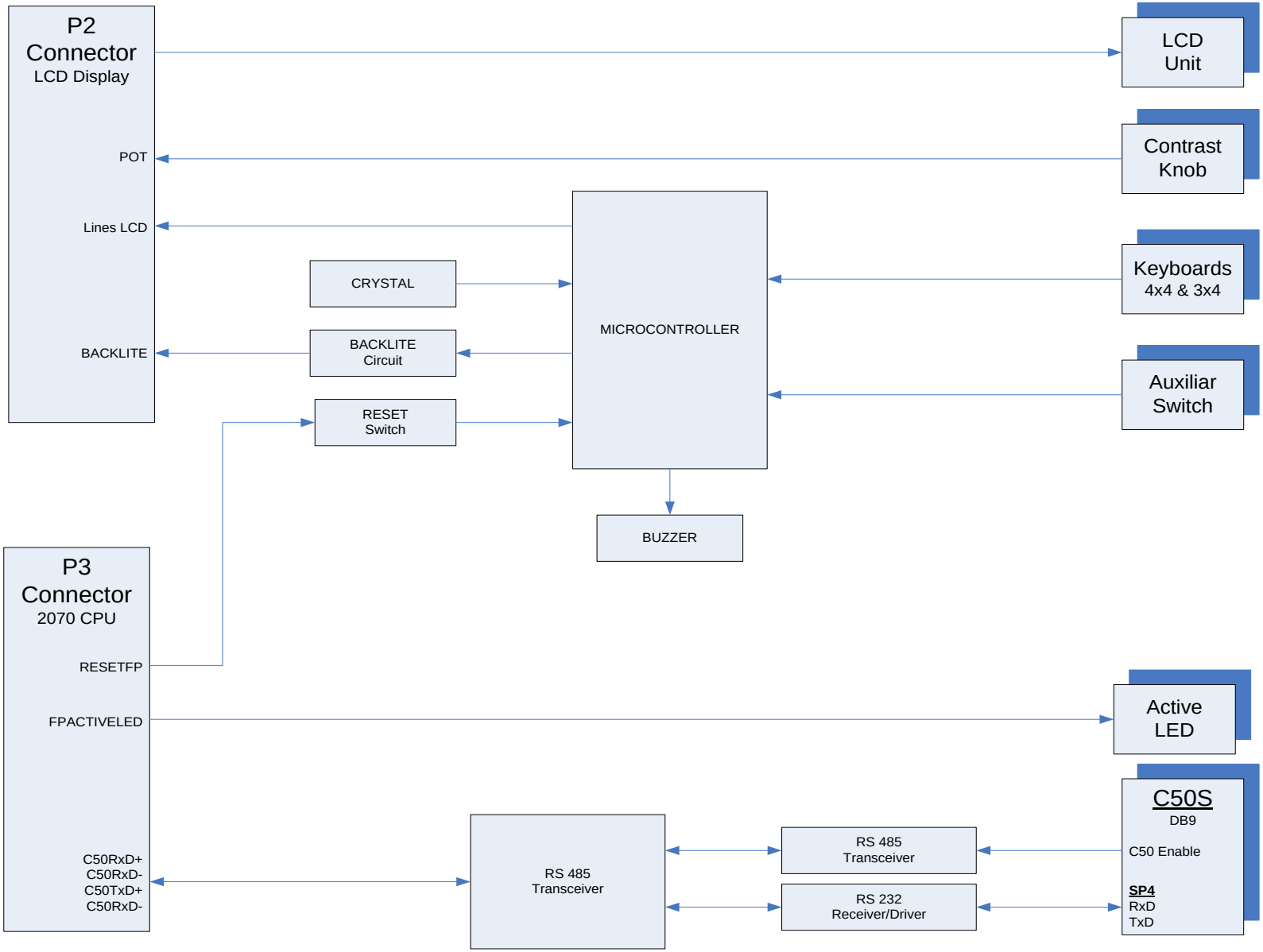
RESET Switch

It is a push-button switch located on the back of the FPA on the PCB sub-assembly. It serves as switch that once touched it momentary pulls down a line monitored by the microcontroller which then reset the operation and also sends a reset the LCD through the P2 connector.

ACTIVE LED

An LED with a series resistor connected to Vcc is activated by the CPU through the P3 connector. This LED is normally used to indicate the status of the application running in the CPU.

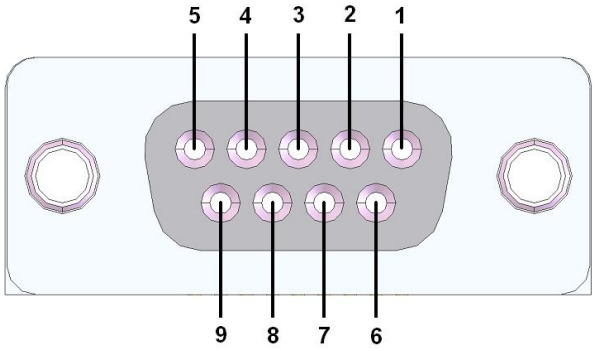
5.3 2070-3A LA CITY BLOCK DIAGRAM



5.4 CONNECTORS' PIN OUT

Connector C50S (DB9 Female):

Pin	Function
1	C50 Enable
2	SP4 RxD
3	SP4 TxD
4	nc
5	DCG #1
6	nc
7	nc
8	nc
9	nc



5.5 2070-3A LA CITY MODULE DIMENSIONS:

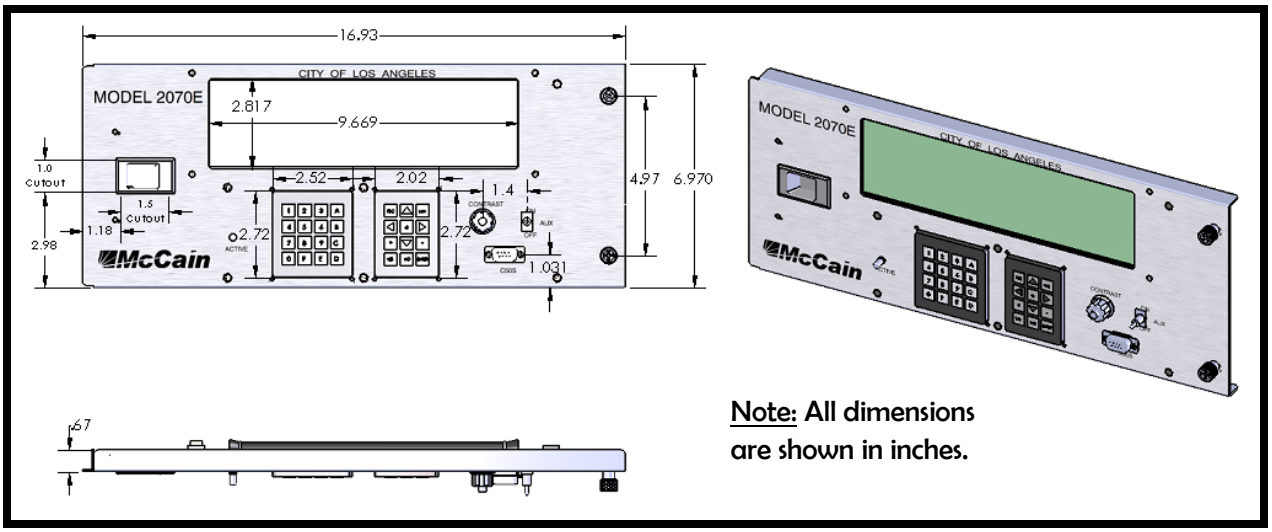


Figure 12: 2070-3A LA City Dimensions

5.6 ADJUSTMENT

The only adjustment available on the Front Panel Assembly is the LCD contrast that can be adjusted in accordance with user's needs through the contrast knob.

5.7 INSTALLING THE 2070-3A LA CITY MODULE

Normally the controller has the 2070-3A LA City assembly, but this section contains information of installation of the 2070-3A LA City in case it is not.

1. Turn off the controller using the power switch located in the front plate of 2070-4A LA City Module.
2. Install on the front of the controller and attach to the chassis' hinge through the two thumbscrews on the right side and secure it through the latch slide on the left side.
3. Tighten the thumbscrews until the module is secure.
4. Insert the 40-position ribbon plug connector from the Serial motherboard into the P3 Connector.
5. Make sure the 2070-3A LA City is correctly opened, closed and secured.

These steps complete the 2070-3A LA City installation in the Controller.

6 2070-4A LA CITY POWER SUPPLY MODULE

6.1 GENERAL DESCRIPTION

The model 2070-4A LA City is the Power Supply module of the Controller. It receives the AC line through the AC cord and provides all necessary power outputs and signal outputs at PS1 and PS2 connectors.

The power lines are +5VDC @ 10A, +/-12VDC @ 0.5A, isolated +12VDC @ 1A and the +5VDC Standby power; and control signals are LINESYNC, ACFAIL/POWER DOWN and POWER UP/SYSTEM RESET.

The module is constructed in accordance to the TEES 2009. It is a self-contained, vented only by convection. The control board and small power supply modules are enclosed by two side plates and one rear plate forming a cage with the top and bottom not covered and used for ventilation purposes.

The Power supply module consists of:

- PS1 and PS2 connectors: Provides the interface for all power and signals needed by the controller.
- LED indicators: They are ON when voltage is within tolerance, otherwise they are OFF.
- ON/OFF Power switch: Provide for turning ON and OFF the module.
- Slow Blow fuse: Provided to protect the module in case of exceeding the current limit.
- 15 inches of AC Cord and cord wraps to stow the cord when not in use.
- A sub-assembly control board: contains all necessary circuitry for implementing the Power Supply module functions.
- Small power supply modules that provide all necessary power.
- Harnessing: for interconnecting the small power modules to the control board.
- Metal panels: provides mechanical support, necessary cutouts and identification.

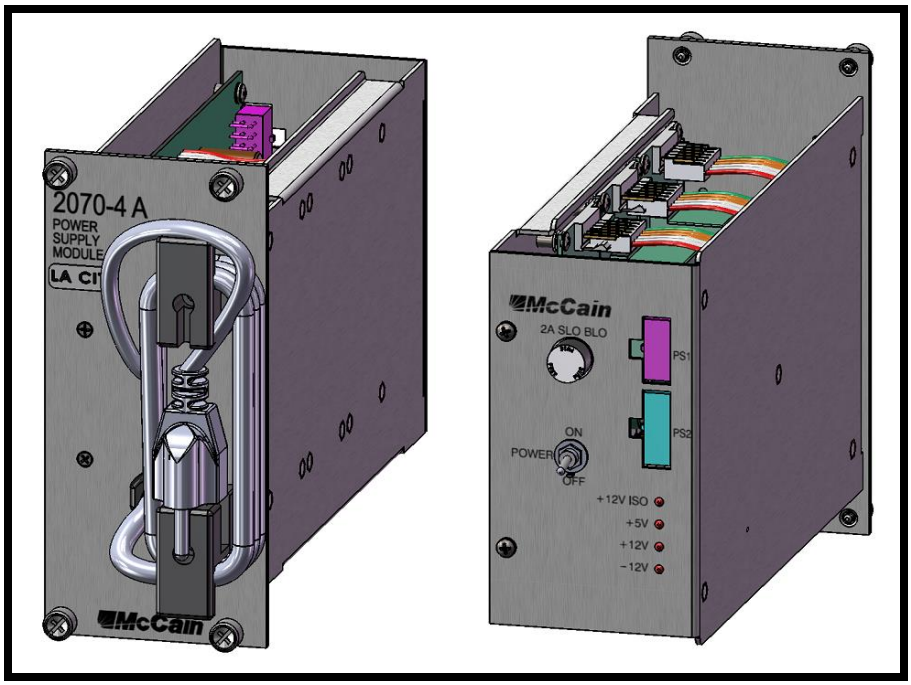


Figure 13: Power Supply 2070-4A LA City

6.2 THEORY OF OPERATION

The 2070-4A LA City Power Supply module consists of several sub-systems that perform different functions in order to meet the requirements listed on TEES 2009.

This section provides a little insight of the sub-systems' functionality.

AC Input, Fuse and Switch

The AC line is fed to the Power Supply from the AC cord to the AC INPUT header providing the Hot, Neutral and Earth lines to the input protection circuitry. The Hot line is routed from the AC INPUT header to the 2A fuse and then to the switch, the next stages are the input protection and the EMI filter.

Input protection

The input protection consists of the next:

- Two 1.5Ohms 15W resistors, one placed on the AC+ line and the other one on the AC- line.
- Three surge arrestors placed between AC+ and AC-, AC+ and EG, AC- and EG.
- One .68uF capacitor located between AC+ and AC-, between the resistors and surge arresters.

EMI Filter

The EMI filter is contained into a discrete device. It receives the AC input signal and delivers the power already filtered to the circuitry in the Power Supply module.

Power Supply Modules

The Power Supply filters the 120 VAC line and then feeds three power modules. These power modules generate the required voltage outputs:

- +5VDC module, is used for providing +5VDC.
- +12VDC module, is used for providing +12VDC and -12VDC (the -12VDC are obtained through a switching regulator on control board).
- +12VDCISO module, is used for providing +12VDCISO.

The Power Supply modules are connected to the Control board via a set of harnesses.

Zero-Crossing Detector circuit

This circuit is based on the MC33161P which is a universal voltage monitor with two comparator channels with hysteresis, a Mode Select Input, a pinned out 2.54V reference and two open collector outputs.

In order to preserve the isolation between the AC and DC signals, a transformer, a diode bridge and an electrolytic capacitor are used to generate 24VDC and feed the circuitry. Also, two opto-isolators MOC8102 are used to isolate the outputs from the AC side to the logic side.

The AC+ line is separated through two resistor networks in order to attenuate it and also to generate a difference on AC voltage levels, and then the AC signal is feed to the inputs of the voltage monitor device as follow:

- Input 1 the resistor network connected to this input is around 510KOhms and it is connected to a 6V zener diode.
- Input 2 the resistor network connected to this input is around 998KOhms and it is connected to a voltage divider in parallel to a 6V zener diode.

The voltage level at one zener feeds a voltage divider including a potentiometer; this voltage divider is very sensitive and sets the trigger level for the comparator at input 2. It is used for factory adjustment to start operation when the AC line reaches the recovery voltage level, for this model 85VAC.

The outputs of the M33161P (OUT1 and OUT2) are routed to two opto-isolators controlling them at the cathode side, so that they are activated according to the zero crossing points of each AC input network. These two isolated signals become the CLOCK and CLEAR signals for the D-Type Flip-Flop whose output is a pulse synchronized to the AC input line called AC monitor.

AC monitor

This signal is generated at the D-type flip-flop which is receiving the alternating signals coming from the opto-isolators at the CLOCK and CLEAR inputs, one input sets the output and the other input clears the output; the generated pulse is synchronized to the AC line because of the zero-crossing detection circuit.

The pulse is monitored by the microcontroller becoming into an interruption, based on the presence or absence of this interruption, the microcontroller generates the control signals LINESYNC, ACFAIL, ACFAIL/PWR DOWN and PWR UP/SYS RESET.

The zero-crossing circuit is adjusted via the potentiometer to obtain this signal while the AC line is above the 85VAC, if the AC line goes below 85VAC then any valid pulse is generated and it is interpreted by the microprocessor as a power failure.

Microcontroller

The Power Supply control is handled by an 8-bit high performance Freescale microcontroller MC9S08QG8 running at 15.36MHz.

The microcontroller has the next tasks:

- Monitors the AC monitor interruption.
- Generate the control signals: ACFAIL/POWERDOWN, POWERUP/SYSTEMRESET and LINESYNC.
- Monitors the voltage levels through three ADC; +5VDC, +12VDC and -12VDC.
- Activates the LED indicators for three voltages; +5VDC, +12VDC and -12VDC.

DC Regulator

A 3.3VDC linear regulator is used in order to feed the microcontroller, oscillator and LED indicators.

Control signals

Upon the arrival of the AC Monitor signal to the microprocessor, it is the firmware that defines if this signal meets the necessary requirements to generate and maintain the control signals ACFAIL/POWERDOWN, POWERUP/SYSTEMRESET and LINESYNC. All these lines are generated by the microprocessor and go to the control signals' output stage.

The ACFAIL/POWER DOWN output lines transition to High at Power Restoration; these lines go Low (ground true) immediately upon Power Failure. These lines are driven separately.

The SYSRESET/POWERUP output Lines go to High 225 ± 25ms after power restoration and the supply is fully recovered; these lines go Low 525 ± 25ms after ACFAIL goes Low.

Power up sequence

After detecting the presence of the AC signal the microcontroller set the ACFAIL/PWR DOWN line to high; if there is no power failure within a 225ms period then the PWR UP/SYS RESET line is set to high.

Power down sequence:

During a power failure, the ACFAIL/PWR DOWN signal is set to Low immediately, if the power failure lasts more than 525 ± 25ms then the PWR UP/SYS RESET line is set to Low.

The LINESYNC signal is a continuous square wave signal of +5VDC amplitude, 8.333 ms half-cycle pulse duration, and 50 ± 1 % duty cycle; it is synchronized to the 60Hz VAC incoming power line at 120 and 300 degree. The LINESYNC signal begins when SYSTEMRESET signal transitions to High; this signal

continues until SYSRESET transitions to Low. The microprocessor compensates for missing pulses during normal operation.

Control signals output stage

It is used for supplying the appropriate drive sink capability to the control signals on the PS connectors. This stage consists of two FET's and three resistors for each control signal, it is arranged for giving an output of the same logic level as the input; this is, if the control signal coming from the microcontrollers is HIGH then the output of this stage is also HIGH.

The Linesync output has a drive sink capability of 16 mA. A 2K ohm pull-up resistor is connected between the output and +5 VDC.

Voltage monitors

In order to monitor the voltage levels for +5VDC, +12VDC and -12VDC voltage dividers are arranged and connected to the microcontroller's ADC's, if the monitored levels are within range the LED status indicators are activated.

Voltage status indicators

A LED status indicator for each power supply is provided to indicate if the voltage levels are within range or not; The LED status indicator is ON if the voltage supply is within range and OFF otherwise: the +5 VDC is within 5% and the 12 VDC is within 8% of their nominal levels.

The LED DC POWER Indicator indicates that the required DC Voltage meets the following conditions: For the +5VDC, +12VDC and -12VDC supplies, the circuit consists of an LED in series with a 220 Ohms resistor, connected to +3.3VDC and activated by the microcontroller.

For the +12VDCISO supply, a discrete voltage monitor device is used. It monitors and indicates if the level is within range. In this case there is an LED with a 2.2KOhms series resistor connected to +12VDCISO and activated by this device.

Standby Power

+ 5 VDC STANDBY POWER is provided to hold up system devices during power down period. It consists of the monitor circuitry; hold up capacitors, and charging circuitry. A charging circuit is provided that under normal operation fully charges and float the capacitors. The Hold Up power requirements are a minimum constant drain of 600uA at a range of +5 to +2 VDC for over 10 hours.

It is achieved through the high efficiency positive voltage regulator ICL7663 and two 47F hold up capacitors plus charging circuitry.

Holdup time

The Power Supply module is able to deliver at least 30W for 550ms after the ACFAIL line is set to Low. It is capable of holding the unit for two 500ms power failure periods occurring in a 1.5 seconds period.

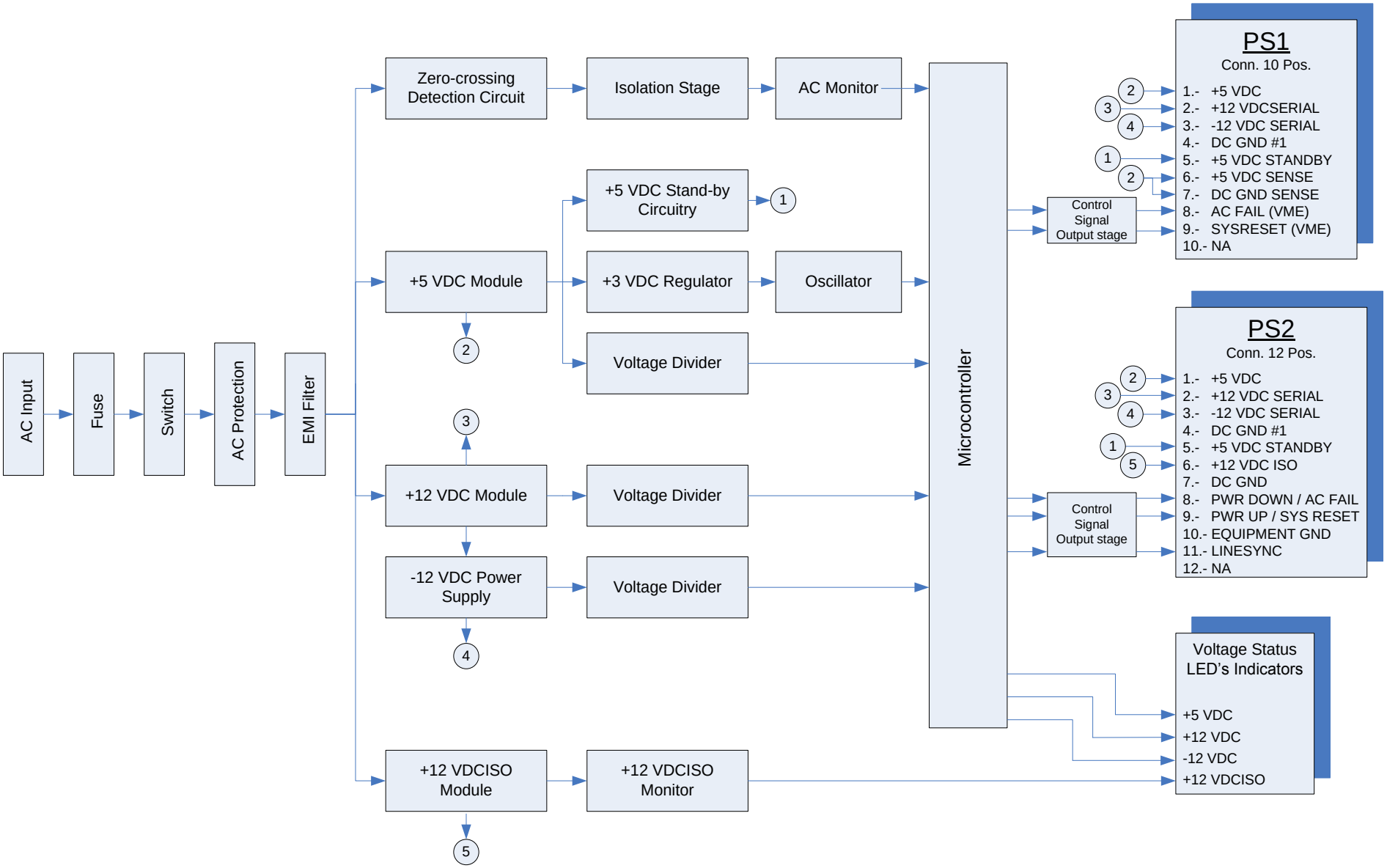
Power Supply requirements

These are the electrical specifications of Power Supply Module.

Voltage	Tolerances	I MIN	I MAX
+5 VDC	+4.875to +5.125 VDC	1.0 AMP	10.0 AMP
+12 VDC Serial	+11.4 to +12.6 VDC	0.1 AMP	0.5 AMP
-12 VDC Serial	-11.4 to –12.6 VDC	0.1 AMP	0.5 AMP
+12 VDC	+11.4 to +12.6 VDC	0.1 AMP	1 AMP

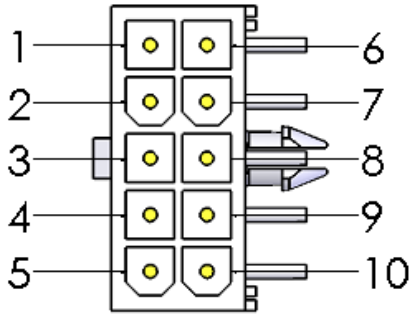
Line / Load Regulation	Meets the table tolerances values for voltage range of 95 to 135 VAC, minimum and maximum loads called out in the table and including ripple noise.
Efficiency	70 % minimum
Ripple & Noise	Less than 0.2 % rms, 1% peak to peak or 50 mV Whichever is greater
Voltage Overshoot	No greater than 5 %, all outputs
Over voltage Protection	130% Vout for all outputs
Inrush Current	Less than 25A at 115 VAC
Transient response	Output voltage returns to within 1% in less than 500 μs on a 50 % Load Change. Peak transient not to exceed 5%
Holdup Time	30 watts minimum for 550mS after ACFAIL goes LOW. The supply is capable of holding up the Unit for two 500ms Power Loss periods occurring in a 1.5 second period.
Remote Sense	+5 VDC compensates 250 mV total line drop. Open sense load protection provided.
Fuse	Value: 2 Amps, Type: 3AG

6.3 2070-4A LA CITY BLOCK DIAGRAM

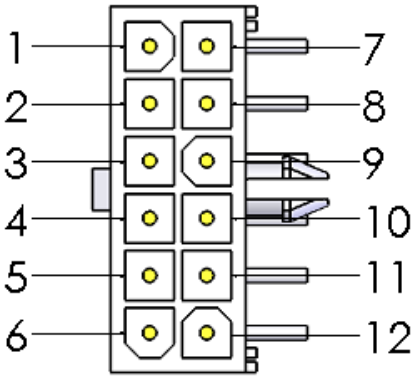


6.4 PS1 AND PS2 CONNECTORS' PIN OUT

PS1 Connector	
Pin	Function
1	+5 VDC
2	+12 VDC SERIAL
3	-12 VDC SERIAL
4	DC GND #1 (+5 VDC & 12 SERIAL)
5	+5 VDC STANDBY
6	+5 VDC SENSE
7	DC GROUND SENSE
8	AC FAIL (VME)
9	SYSRESET (VME)
10	nc



PS2 Connector	
Pin	Function
1	+5 VDC
2	+12 VDC SERIAL
3	-12 VDC SERIAL
4	DC GND #1 (+5 VDC & 12 SERIAL)
5	+5 VDC STANDBY
6	+12 VDC ISO
7	DC GND (+12 VDC ONLY)
8	POWER DOWN / AC FAIL
9	POWER UP / SYS RESET
10	EQUIPMENT GROUND
11	LINESYNC
12	nc



6.5 2070-4A LA CITY MODULE DIMENSIONS

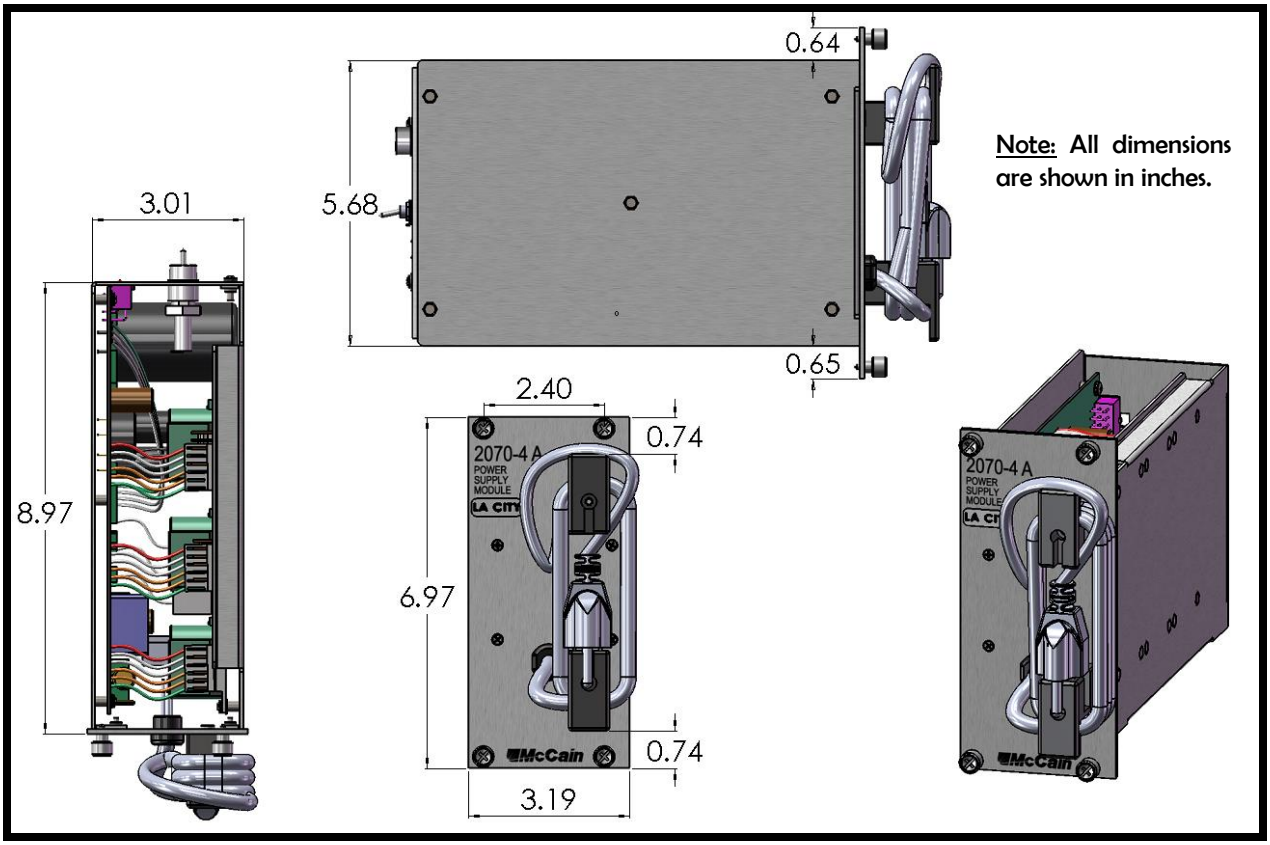


Figure 14: 2070-4A LA City Dimensions

6.6 ADJUSTMENT

There are four factory set adjustments of the Power Supply module and must not be moved.

One adjustment corresponds to the AC line voltage window:

- Power Fail: 92VAC ±2VAC.
- Power Recovery: 97VAC ±2VAC.

This is done via a potentiometer located at the edge of the Control board.

One adjustment is performed for each power module to be set at the DC voltage level required. This is done via a potentiometer located at each power module.

INSTALLING THE 2070-4A LA CITY MODULE

Normally the controller has the 2070-4A LA City module, but this section contains information of installation of the 2070-4A LA City in case it is not.

1. Turn off the 2070-4A LA City module before the installation. Turn the Power switch OFF.
2. Slide the module into its corresponding compartment from the back of the Chassis unit and attach it by tightening its four TSD #3 devices.
3. Plug the PS2 harness coming from the Serial motherboard.
4. Plug the AC cord into its corresponding AC outlet.
5. Turn the 2070-4A LA City module on. Turn the Power switch ON.

These steps complete the 2070-4A LA City installation into the Controller.

7 CHASSIS UNIT

7.1 GENERAL DESCRIPTION

The chassis unit is an aluminum enclosure that serves for containing and interconnecting the different 2070's modules depending on the selected configuration. It supports the installation of optional modules; for example, a power supply module, a front panel module, a CPU module, a Field I/O module, and two communications boards (modems, GPS, synchronous and/or asynchronous boards, etc); also blank filler plates can be installed for unused slots.

Chassis unit is designed to be convection cooled via vertical ventilation using slots in the top and bottom plates.

It can be shelf mounted or rack mounted with 170 CALTRANS facilities.

The chassis unit consists of:

- Top and bottom sides have slots for convection cooling and flushed nuts for accepting the thumbscrews of the modules to be installed; also they have flushed nut for installing the serial motherboard. Left side and right side have provisions for installing the hinge and latch and also for allowing the controller to be rack mounted.
- Screws are stainless steel, countersunk, Phillips, flat head, except for the ones for holding the serial mother board which are pan head.
- Serial motherboard with a wiring harness to be plugged to power supply PS2 receptacle connector and five DIN-96 receptacle connectors labeled as A1 to A5 for plugging optional modules.
- Card guides on top and bottom sides to allow modules slide and plug to the serial motherboard and also for installing the power supply module.
- The hinge on right side and latch on left side to hold and secure the front panel assembly.

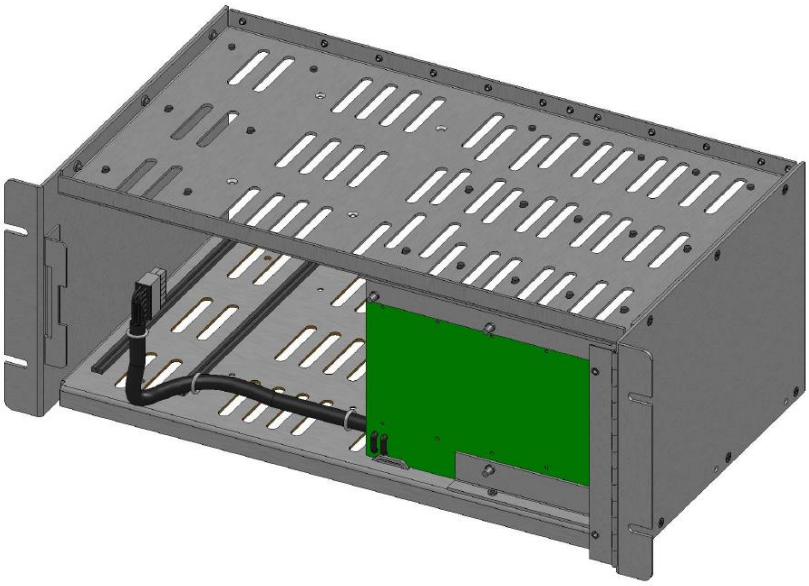
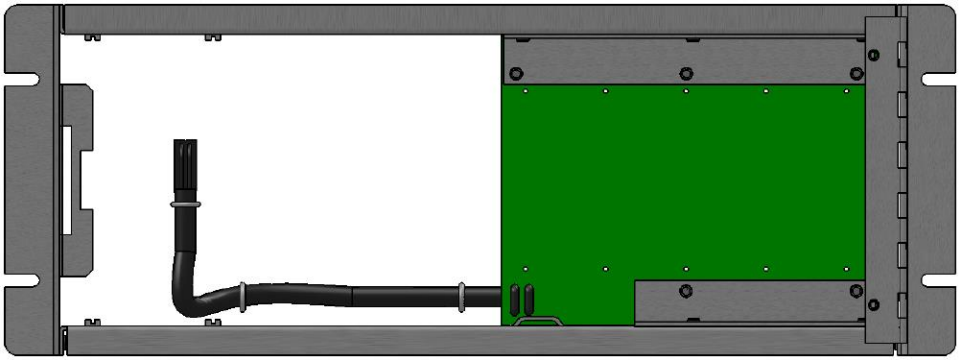
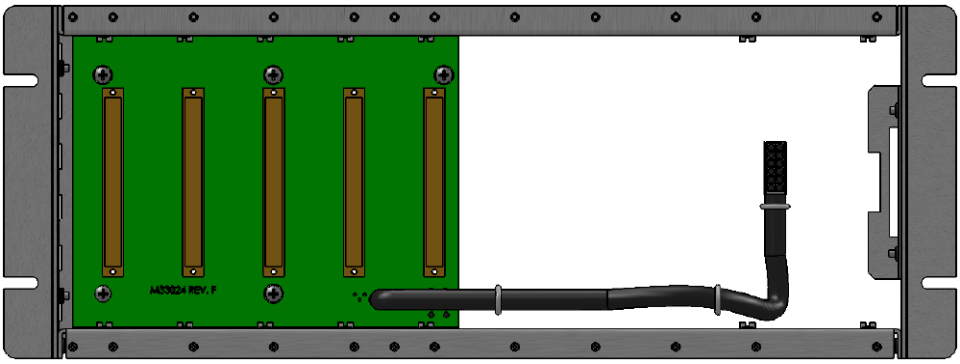


Figure 15: 2070E Chassis unit



Chassis front view



Chassis rear view

Figure 16: Front and rear view 2070E Chassis

7.2 SERIAL MOTHERBOARD

7.2.1 Theory of operation

The Serial Motherboard (Back plane) is a PCB sub-assembly that provides the interconnection of power lines and signals of the modules installed into the 2070 chassis. This means that it provides the buses for power, control and communication signals among the modules installed into slots A1 to A5, power supply and front panel.

The serial motherboard consists of:

- A multilayered PCB that provide the necessary interconnections among the connectors to be soldered to it.
- Five 96-positions DIN receptacle connectors labeled as A1 to A5 for plugging optional modules.
- A wiring harness to be plugged to power supply PS2 receptacle connector. It is soldered at PCB side, braided, tightened with wire ties and finished with crimped gold sockets loaded into a 12-positions plug connector.
- A 40-positions flat ribbon cable harness for connecting to the front panel module. It is soldered to the PCB side and finished with a 40-positions keyed plug receptacle.
- Support brackets with flushed nuts installed to be attached to the top and bottom sides of the chassis.
- Stainless steel, Phillips, pan head screws and washers; they are used to attach the brackets to the PCB and to the chassis.

The Motherboard receives power and control signals from the PS2 connector on power supply through the wiring harness soldered to the PCB; then Motherboard distributes the power and control signals to the five 96-pin DIN connectors and to the connector dedicated to the front panel interface. It also carries the serial communication among the dedicated modules and front panel module.

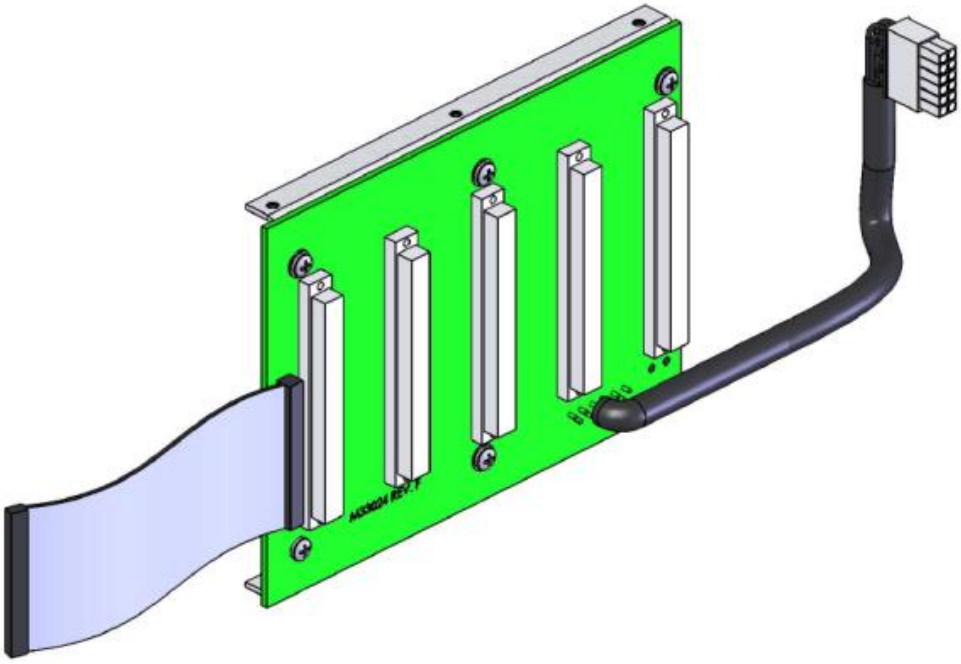
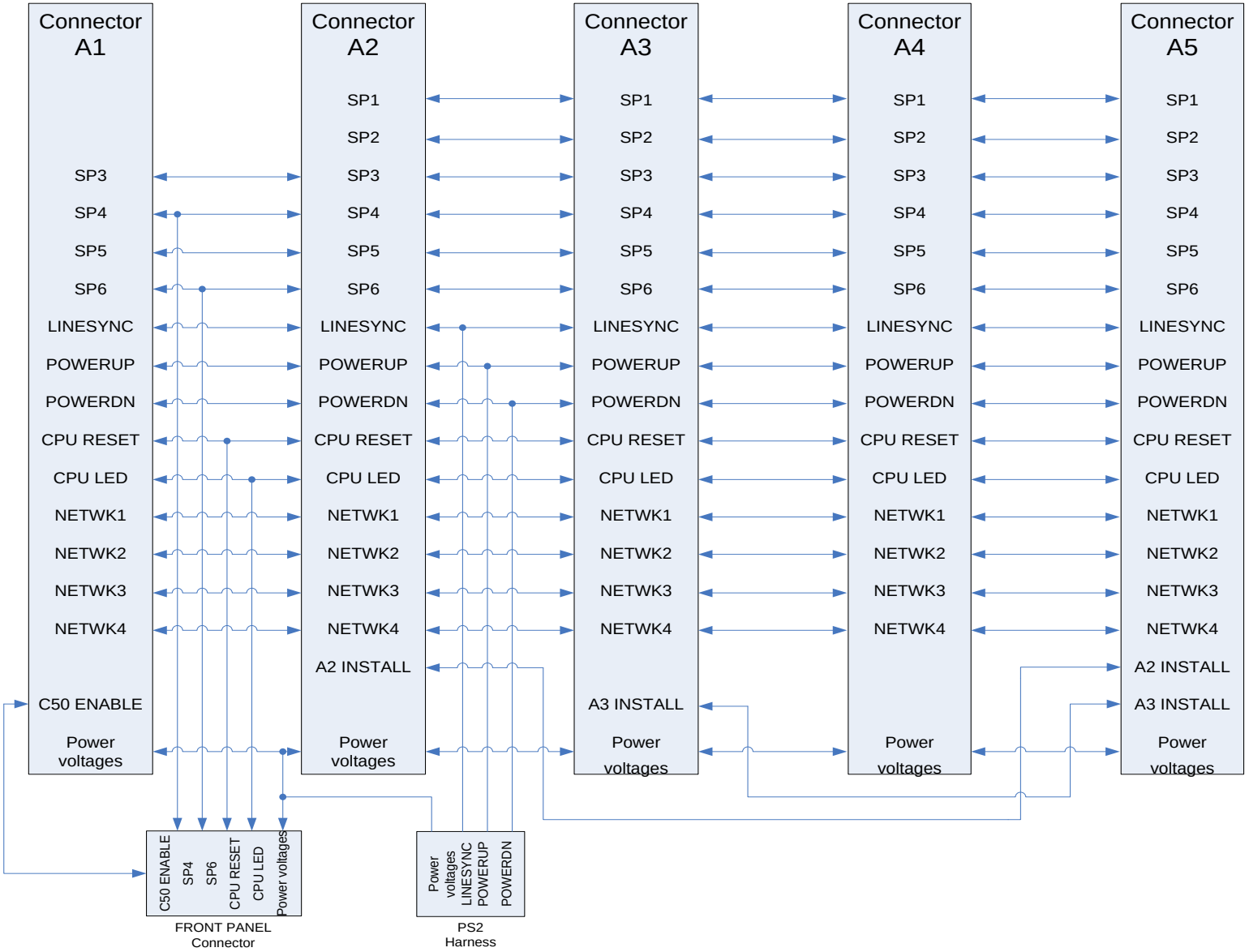


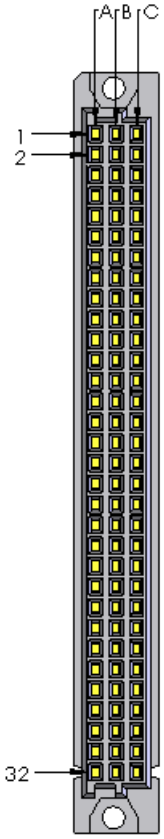
Figure 17: 2070 Serial motherboard

7.3 2070 SERIAL MOTHERBOARD BLOCK DIAGRAM

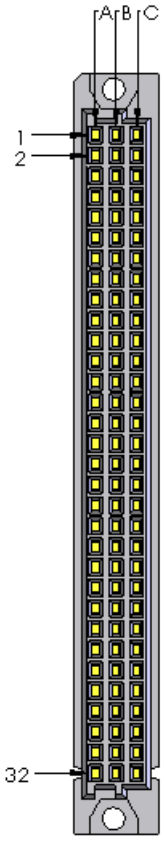


7.4 CONNECTORS' PIN OUT:

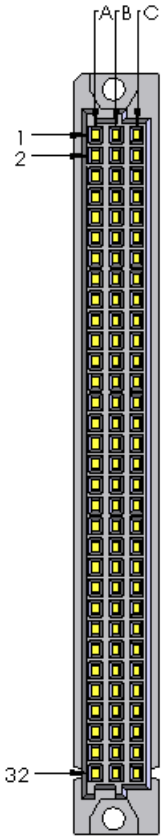
A1 Connector					
Pin	Function	Pin	Function	Pin	Function
A1	SP3TXD+	B1	SP6TXD+	C1	SP5TXD+
A2	SP3TKD-	B2	SP6TXD-	C2	SP5TXD-
A3	SP3RXD+	B3	SP6RXD+	C3	SP5TXC+
A4	SP3RXD-	B4	SP6RXD-	C4	SP5TXC-
A5	SP3RTS+	B5	SP3TXCO+	C5	SP5RXD+
A6	SP3RTS-	B6	SP3TXCO-	C6	SP5RXD-
A7	SP3CTS+	B7	SP3TXCI+	C7	SP5RXC+
A8	SP3CTS-	B8	SP3TXCI-	C8	SP5RXC-
A9	SP3DCD+	B9	SP3RXC+	C9	SP3TXD+
A10	SP3DCD-	B10	SP3RXC-	C10	SP3TXD-
A11	SP4TXD+	B11	SP4TXD+	C11	SP3RXD+
A12	SP4TXD-	B12	SP4TXD-	C12	SP3RXD-
A13	SP4RXD+	B13	SP4RXD+	C13	SP3RTS+
A14	SP4RXD-	B14	SP4RXD-	C14	SP3RTS-
A15	~	B15	~	C15	SP3CTS+
A16	~	B16	~	C16	SP3CTS-
A17	~	B17	~	C17	SP3DCD+
A18	~	B18	~	C18	SP3DCD-
A19	~	B19	~	C19	SP3TXCO+
A20	~	B20	~	C20	SP3TXCO-
A21	DCG#1	B21	C50ENABLE	C21	SP3TXCI+
A22	NETWK1	B22	~	C22	SP3RXCI-
A23	NETWK2	B23	~	C23	SP3RXC+
A24	~	B24	LINESYNC	C24	SP3RXC-
A25	NETWK3	B25	POWERUP	C25	CPURESET
A26	NETWK4	B26	POWERDOWN	C26	CPU LED
A27	DCG#1	B27	DCG#1	C27	DCG#1
A28	+12VDCSERIAL	B28	-12VDCSERIAL	C28	+5VDCSTANDBY
A29	5VDC	B29	+5VDC	C29	+5VDC
A30	DCG#1	B30	DCG#1	C30	DCG#1
A31	+12VDC	B31	+12VDC	C31	+12VDC
A32	DCG#2	B32	DCG#2	C32	DCG#2



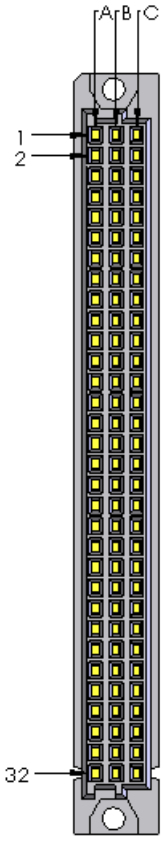
A2 Connector					
Pin	Function	Pin	Function	Pin	Function
A1	SP1TXD+	B1	SP6TXD+	C1	SP5TXD+
A2	SP1TKD-	B2	SP6TXD-	C2	SP5TXD-
A3	SP1RXD+	B3	SP6RXD+	C3	SP5TXC+
A4	SP1RXD-	B4	SP6RXD-	C4	SP5TXC-
A5	SP1RTS+	B5	SP1TXCO+	C5	SP5RXD+
A6	SP1RTS-	B6	SP1TXCO-	C6	SP5RXD-
A7	SP1CTS+	B7	SP1TXCI+	C7	SP5RXC+
A8	SP1CTS-	B8	SP1TXCI-	C8	SP5RXC-
A9	SP1DCD+	B9	SP1RXC+	C9	SP3TXD+
A10	SP1DCD-	B10	SP1RXC-	C10	SP3TXD-
A11	SP2TXD+	B11	SP4TXD+	C11	SP3RXD+
A12	SP2TXD-	B12	SP4TXD-	C12	SP3RXD-
A13	SP2RXD+	B13	SP4RXD+	C13	SP3RTS+
A14	SP2RXD-	B14	SP4RXD-	C14	SP3RTS-
A15	SP2RTS+	B15	SP2TXCO+	C15	SP3CTS+
A16	SP2RTS-	B16	SP2TXCO-	C16	SP3CTS-
A17	SP2CTS+	B17	SP2TXCI+	C17	SP3DCD+
A18	SP2CTS-	B18	SP2TXCI-	C18	SP3DCD-
A19	SP2DCD+	B19	SP2RXC+	C19	SP3TXCO+
A20	SP2DCD-	B20	SP2RXC-	C20	SP3TXCO-
A21	DCG#1	B21	~	C21	SP3TXCI+
A22	NETWK1	B22	~	C22	SP3RXCI-
A23	NETWK2	B23	A2INSTALLED	C23	SP3RXC+
A24	~	B24	LINESYNC	C24	SP3RXC-
A25	NETWK3	B25	POWERUP	C25	CPURESET
A26	NETWK4	B26	POWERDOWN	C26	CPU LED
A27	DCG#1	B27	DCG#1	C27	DCG#1
A28	+12VDCSERIAL	B28	-12VDCSERIAL	C28	+5VDCSTANDBY
A29	5VDC	B29	+5VDC	C29	+5VDC
A30	DCG#1	B30	DCG#1	C30	DCG#1
A31	+12VDC	B31	+12VDC	C31	+12VDC
A32	DCG#2	B32	DCG#2	C32	DCG#2



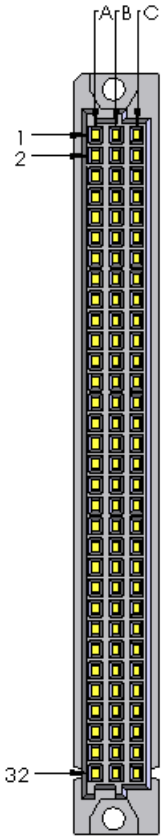
A3 Connector					
Pin	Function	Pin	Function	Pin	Function
A1	SP1TXD+	B1	SP6TXD+	C1	SP5TXD+
A2	SP1TKD-	B2	SP6TXD-	C2	SP5TXD-
A3	SP1RXD+	B3	SP6RXD+	C3	SP5TXC+
A4	SP1RXD-	B4	SP6RXD-	C4	SP5TXC-
A5	SP1RTS+	B5	SP1TXCO+	C5	SP5RXD+
A6	SP1RTS-	B6	SP1TXCO-	C6	SP5RXD-
A7	SP1CTS+	B7	SP1TXCI+	C7	SP5RXC+
A8	SP1CTS-	B8	SP1TXCI-	C8	SP5RXC-
A9	SP1DCD+	B9	SP1RXC+	C9	SP3TXD+
A10	SP1DCD-	B10	SP1RXC-	C10	SP3TXD-
A11	SP2TXD+	B11	SP4TXD+	C11	SP3RXD+
A12	SP2TXD-	B12	SP4TXD-	C12	SP3RXD-
A13	SP2RXD+	B13	SP4RXD+	C13	SP3RTS+
A14	SP2RXD-	B14	SP4RXD-	C14	SP3RTS-
A15	SP2RTS+	B15	SP2TXCO+	C15	SP3CTS+
A16	SP2RTS-	B16	SP2TXCO-	C16	SP3CTS-
A17	SP2CTS+	B17	SP2TXCI+	C17	SP3DCD+
A18	SP2CTS-	B18	SP2TXCI-	C18	SP3DCD-
A19	SP2DCD+	B19	SP2RXC+	C19	SP3TXCO+
A20	SP2DCD-	B20	SP2RXC-	C20	SP3TXCO-
A21	DCG#1	B21	~	C21	SP3TXCI+
A22	NETWK1	B22	~	C22	SP3RXCI-
A23	NETWK2	B23	A3INSTALLED	C23	SP3RXC+
A24	~	B24	LINESYNC	C24	SP3RXC-
A25	NETWK3	B25	POWERUP	C25	CPURESET
A26	NETWK4	B26	POWERDOWN	C26	CPU LED
A27	DCG#1	B27	DCG#1	C27	DCG#1
A28	+12VDCSERIAL	B28	-12VDCSERIAL	C28	+5VDCSTANDBY
A29	5VDC	B29	+5VDC	C29	+5VDC
A30	DCG#1	B30	DCG#1	C30	DCG#1
A31	+12VDC	B31	+12VDC	C31	+12VDC
A32	DCG#2	B32	DCG#2	C32	DCG#2



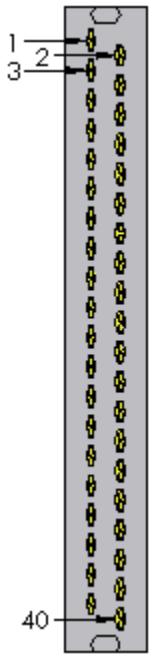
A4 Connector					
Pin	Function	Pin	Function	Pin	Function
A1	SP1TXD+	B1	SP6TXD+	C1	SP5TXD+
A2	SP1TKD-	B2	SP6TXD-	C2	SP5TXD-
A3	SP1RXD+	B3	SP6RXD+	C3	SP5TXC+
A4	SP1RXD-	B4	SP6RXD-	C4	SP5TXC-
A5	SP1RTS+	B5	SP1TXCO+	C5	SP5RXD+
A6	SP1RTS-	B6	SP1TXCO-	C6	SP5RXD-
A7	SP1CTS+	B7	SP1TXCI+	C7	SP5RXC+
A8	SP1CTS-	B8	SP1TXCI-	C8	SP5RXC-
A9	SP1DCD+	B9	SP1RXC+	C9	SP3TXD+
A10	SP1DCD-	B10	SP1RXC-	C10	SP3TXD-
A11	SP2TXD+	B11	SP4TXD+	C11	SP3RXD+
A12	SP2TXD-	B12	SP4TXD-	C12	SP3RXD-
A13	SP2RXD+	B13	SP4RXD+	C13	SP3RTS+
A14	SP2RXD-	B14	SP4RXD-	C14	SP3RTS-
A15	SP2RTS+	B15	SP2TXCO+	C15	SP3CTS+
A16	SP2RTS-	B16	SP2TXCO-	C16	SP3CTS-
A17	SP2CTS+	B17	SP2TXCI+	C17	SP3DCD+
A18	SP2CTS-	B18	SP2TXCI-	C18	SP3DCD-
A19	SP2DCD+	B19	SP2RXC+	C19	SP3TXCO+
A20	SP2DCD-	B20	SP2RXC-	C20	SP3TXCO-
A21	DCG#1	B21	~	C21	SP3TXCI+
A22	NETWK1	B22	~	C22	SP3RXCI-
A23	NETWK2	B23	~	C23	SP3RXC+
A24	~	B24	LINESYNC	C24	SP3RXC-
A25	NETWK3	B25	POWERUP	C25	CPURESET
A26	NETWK4	B26	POWERDOWN	C26	CPU LED
A27	DCG#1	B27	DCG#1	C27	DCG#1
A28	+12VDCSERIAL	B28	-12VDCSERIAL	C28	+5VDCSTANDBY
A29	5VDC	B29	+5VDC	C29	+5VDC
A30	DCG#1	B30	DCG#1	C30	DCG#1
A31	+12VDC	B31	+12VDC	C31	+12VDC
A32	DCG#2	B32	DCG#2	C32	DCG#2



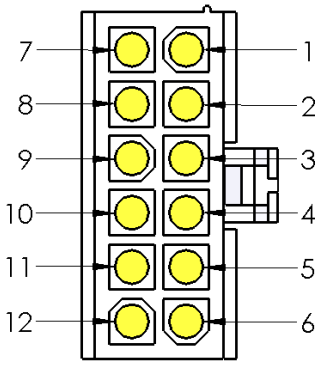
A5 Connector					
Pin	Function	Pin	Function	Pin	Function
A1	SP1TXD+	B1	SP6TXD+	C1	SP5TXD+
A2	SP1TKD-	B2	SP6TXD-	C2	SP5TXD-
A3	SP1RXD+	B3	SP6RXD+	C3	SP5TXC+
A4	SP1RXD-	B4	SP6RXD-	C4	SP5TXC-
A5	SP1RTS+	B5	SP1TXCO+	C5	SP5RXD+
A6	SP1RTS-	B6	SP1TXCO-	C6	SP5RXD-
A7	SP1CTS+	B7	SP1TXCI+	C7	SP5RXC+
A8	SP1CTS-	B8	SP1TXCI-	C8	SP5RXC-
A9	SP1DCD+	B9	SP1RXC+	C9	SP3TXD+
A10	SP1DCD-	B10	SP1RXC-	C10	SP3TXD-
A11	SP2TXD+	B11	SP4TXD+	C11	SP3RXD+
A12	SP2TXD-	B12	SP4TXD-	C12	SP3RXD-
A13	SP2RXD+	B13	SP4RXD+	C13	SP3RTS+
A14	SP2RXD-	B14	SP4RXD-	C14	SP3RTS-
A15	SP2RTS+	B15	SP2TXCO+	C15	SP3CTS+
A16	SP2RTS-	B16	SP2TXCO-	C16	SP3CTS-
A17	SP2CTS+	B17	SP2TXCI+	C17	SP3DCD+
A18	SP2CTS-	B18	SP2TXCI-	C18	SP3DCD-
A19	SP2DCD+	B19	SP2RXC+	C19	SP3TXCO+
A20	SP2DCD-	B20	SP2RXC-	C20	SP3TXCO-
A21	DCG#1	B21	A2INSTALLED	C21	SP3TXCI+
A22	NETWK1	B22	DCG#1	C22	SP3RXCI-
A23	NETWK2	B23	A3INSTALLED	C23	SP3RXC+
A24	~	B24	LINESYNC	C24	SP3RXC-
A25	NETWK3	B25	POWERUP	C25	CPURESET
A26	NETWK4	B26	POWERDOWN	C26	CPU LED
A27	DCG#1	B27	DCG#1	C27	DCG#1
A28	+12VDCSERIAL	B28	-12VDCSERIAL	C28	+5VDCSTANDBY
A29	5VDC	B29	+5VDC	C29	+5VDC
A30	DCG#1	B30	DCG#1	C30	DCG#1
A31	+12VDC	B31	+12VDC	C31	+12VDC
A32	DCG#2	B32	DCG#2	C32	DCG#2



Front Panel Connector			
Pin	Function	Pin	Function
1	SP4TXD+	2	SP4TXD-
3	SP4RXD+	4	SP4RXD-
5	SP6TXD+	6	SP6TXD-
7	SP6RXD+	8	SP6RXD-
9	~	10	~
11	~	12	~
13	~	14	~
15	~	16	~
17	~	18	~
19	~	20	~
21	DCG#1	22	DCG#1
23	+12VDCSERIAL	24	-12VDCSERIAL
25	DCG#1	26	DCG#1
27	CPU LED	28	DCG#1
29	CPURESET	30	DCG#1
31	DCG#1	32	C50ENABLE
33	DCG#1	34	+5VDC
35	+5VDC	36	+5VDC
37	+5VDC	38	+5VDC
39	~	40	~



PS2 Connector			
Pin	Function	Pin	Function
1	+5VDC	7	DCG#2
2	+12VDCSERIAL	8	POWERDOWN
3	-12VDCSERIAL	9	POWERUP
4	DCG#1	10	EQUIPMENT GROUND
5	+5VDCSTANDBY	11	LINESYNC
6	+12VDC	12	DCG#1



8 GENERAL SPECIFICATIONS

Style: Caltrans 2070

Dimensions: 7” H x 19” W x 13” D (rounded to the nearest inch)

Form factor: Shelf mount or 19” EIA (Electronics Industry Alliance) rack mount

Weight: ± 12.7 lbs (based on final module selection)

Power:

AC voltage: 85 VAC to 135 VAC

Frequency: 60 Hz (± 3 Hz)

Power supply output specifications:

+5.0 VDC: 1.0 A - 10.0 A

+12.0 VDC Serial: 0.1 A - 0.5 A

–12.0 VDC Serial: 0.1 A - 0.5 A

+12.0 VDC ISO: 0.1 A - 1.0 A

Environment:

Operating Temperature: -37° C to +74° C

Humidity: 0 to 95% (non-condensing)