2070LX

Controller

USER MANUAL

Version: 1.0

Product Part Number: M54372

Product specifications: www.mccain-inc.com

Customer support: support@mccain-inc.com

Product Inquiries: 888-2-McCain (888-262-2246)

This page was intentionally left blank

REVISIONS			
Rev	**By**	**Date**	**Comments**
1.0	A. Lozoya	Oct/29/2015	Initial Release

DISCLAIMERS

User Responsibility

This document is subject to revision. Users of this document are responsible for verifying the current version status before using this document and or discarding all older revisions.

McCain Inc. shall not be liable for errors contained herein or for incidental or consequential damages in connection with furnishing, performance or use of this material. MCCAIN MAKES NO WARRANTY OF ANY KIND WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

McCain Inc. // 2365 Oak Ridge Way // Vista, CA 92081
PH 760-727-8100

Product Specifications: www.mccain-inc.com
Customer Support: support@mccain-inc.com
Product Inquiries: 888-2-McCain (888-262-2246)

Table of Contents

1 2070LX CONTROLLER 1

1.1 Product description 1
1.2 Benefits 1
1.3 Configuration 1
1.4 Standard features 4
1.5 Interfaces 4

2 2070-1C CPU MODULE 5

2.1 General description 5
2.2 Standard features 6
2.3 Communication interfaces' description 6
2.4 Theory of operation 11
2.4.1 Host board 11
2.4.1.1 The DIN-96 Connector 11
2.4.1.2 C13S Connector circuitry 11
2.4.1.3 Control signals circuit 12
2.4.1.4 Receptacles for engine board installation 12
2.4.1.5 RS-485 line driver/receivers circuitry 12
2.4.1.6 Back up circuitry 13
2.4.1.7 Ethernet switches 13
2.4.1.8 USB Hub 14
2.4.1.9 Datakey circuitry 15
2.4.1.10 ACTIVE LED circuit 15
2.4.1.11 A2-A3 installation detection circuitry 15
2.4.1.12 SD CARD Circuit 16
2.4.2 Engine Board 16
2.4.2.1 Microprocessor 16
2.4.2.2 Memory 17
2.4.2.3 Communications 17
2.4.2.4 Reset management 18
2.4.2.5 Support circuitry 18
2.4.2.6 Reset Circuits 21
2.5 2070LX Hostboard and Engine Block Diagrams 25
2.6 Connectors' Pin Out 29

2.7 2070-1C module dimensions....32
2.8 Adjustment....32
2.9 Installing the 2070-1C CPU Module....32
3 2070-2E+ FIELD I/O MODULE....33
3.1 General description....33
3.2 Theory of operation....34
3.3 2070-2E+ Block Diagram....40
3.4 Connectors' Pin Out....42
3.5 2070-2E+ module dimensions....44
3.6 Installing the 2070-2E+ Module....44
4 2070LX MODULE, FRONT PANEL ASSEMBLY....45
4.1 General description....45
4.2 Theory of operation....46
4.3 2070LX Block Diagram....48
4.4 Connectors' Pin Out....49
4.5 2070LX module dimensions....49
4.6 Adjustment....50
4.7 Installing the 2070LX....50
5 2070-4A POWER SUPPLY MODULE....51
5.1 General description....51
5.2 Theory of operation....52
5.3 2070-4A Block Diagram....57
5.4 PS1 and PS2 Connectors' Pin Out....58
5.5 2070-4A module dimensions....59
5.6 Adjustment....59
5.7 Installing the 2070-4A module....60
6 CHASSIS UNIT....61
6.1 General description....61
6.2 Serial Motherboard....63
6.2.1 Theory of operation....63
6.3 2070 Serial Motherboard Block Diagram....64
6.4 Connectors' Pin Out....65
7 GENERAL SPECIFICATIONS....71

Table of Figures

Figure 1: 2070LX Controller, Front and Rear Views 2
Figure 2: 2070LX Controller System Configuration 3
Figure 3: 2070-1C CPU Module 5
Figure 4: 2070-1C CPU dimensions. 32
Figure 5: 2070-2E+ Module 33
Figure 6: 2070-2E+ Dimensions 44
Figure 7: 2070LX Module 45
Figure 8: 2070LX Dimensions 49
Figure 9: Power Supply 2070-4A 51
Figure 10: 2070-4A Dimensions 59
Figure 11: 2070LX Chassis unit 61
Figure 12: Front and rear view 2070LX Chassis 62
Figure 13: 2070 Serial motherboard 63

This page was intentionally left blank

1 2070LX CONTROLLER

1.1 PRODUCT DESCRIPTION

The 2070LX Controller is a ruggedized, multitasking field processor and communications system that is easily configurable for a variety of traffic management applications in either a rack or shelf mount configuration.

The 2070LX Controller has a general purpose nature, open architecture and modular design, and its functionality depends on the software loaded into the controller and the modules included.

McCain's 2070LX Controller, is designed in full compliance with Caltrans Transportation Electrical Equipment Specifications (TEES) 2009.

The McCain's 2070LX Controller's primary function is intersection control but can be used for a multitude of applications based on the controller's software.

The controller's Linux operating system provides a robust, flexible and expandable platform that is compatible with multi-vendor application control software.

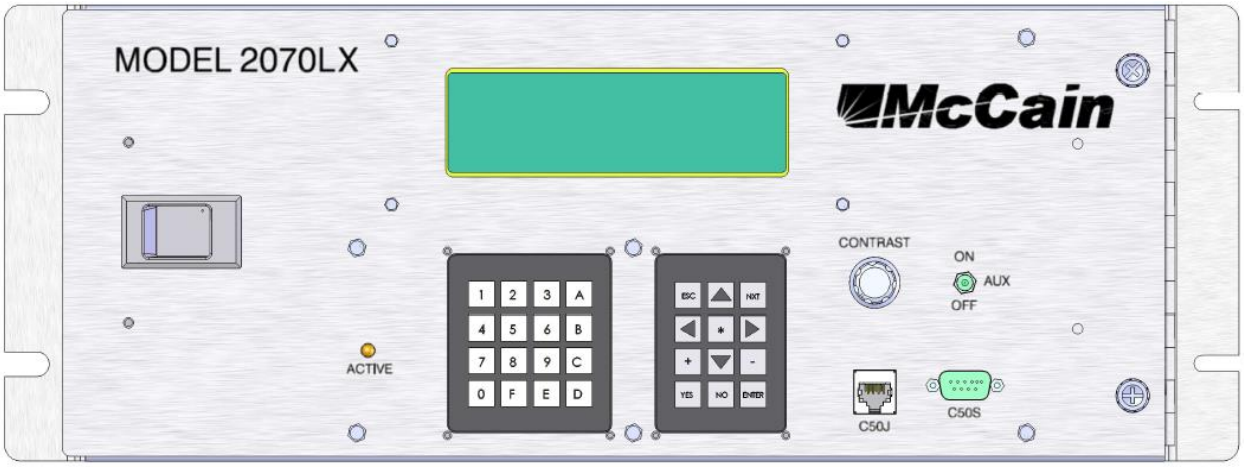
1.2 BENEFITS

- Open Architecture insures compatibility with off-the-shelf products Linux Software – Standard Software Modules from Multiple Sources.
- Flexible Design to Meet Specific User Needs.
- The controller's multitasking operating system (OS) supports a variety of applications.
- Easily upgrades current intersection hardware.
- Multitasking – Each 2070LX Unit Can Control Multiple Applications.
- Physically Compatible with Model 170&170E Controllers & Facilities.

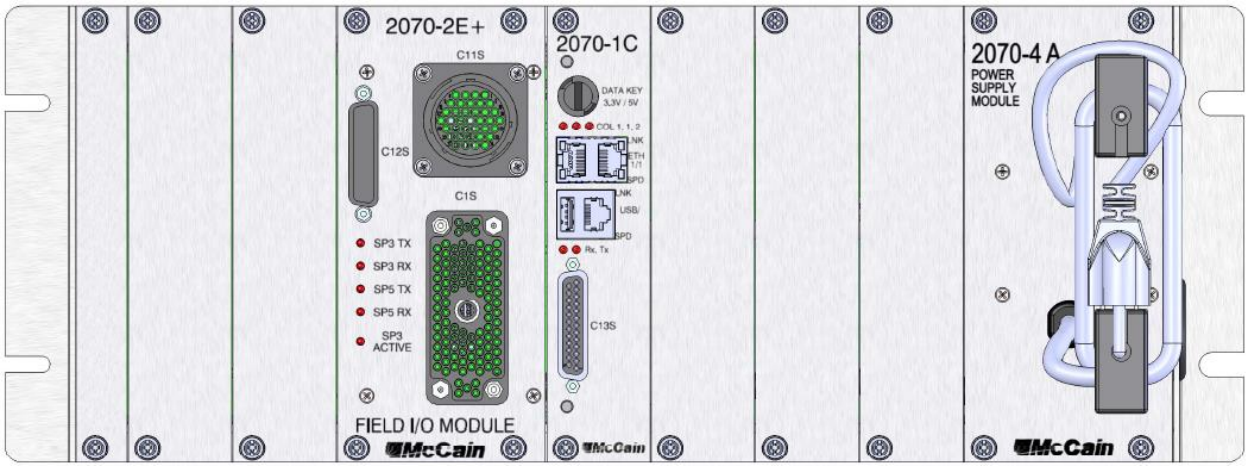
1.3 CONFIGURATION

This controller configuration is constructed as follows (See Figure 1):

- 2070E Chassis unit.
- 2070-1C CPU module.
- 2070-2E+ Field I/O module.
- 2070LX Front Panel module.
- 2070-4A Power Supply module.
- Blank filler plates: There are five 2X and one 1X.



FRONT VIEW



REAR VIEW

Figure 1: 2070LX Controller, Front and Rear Views

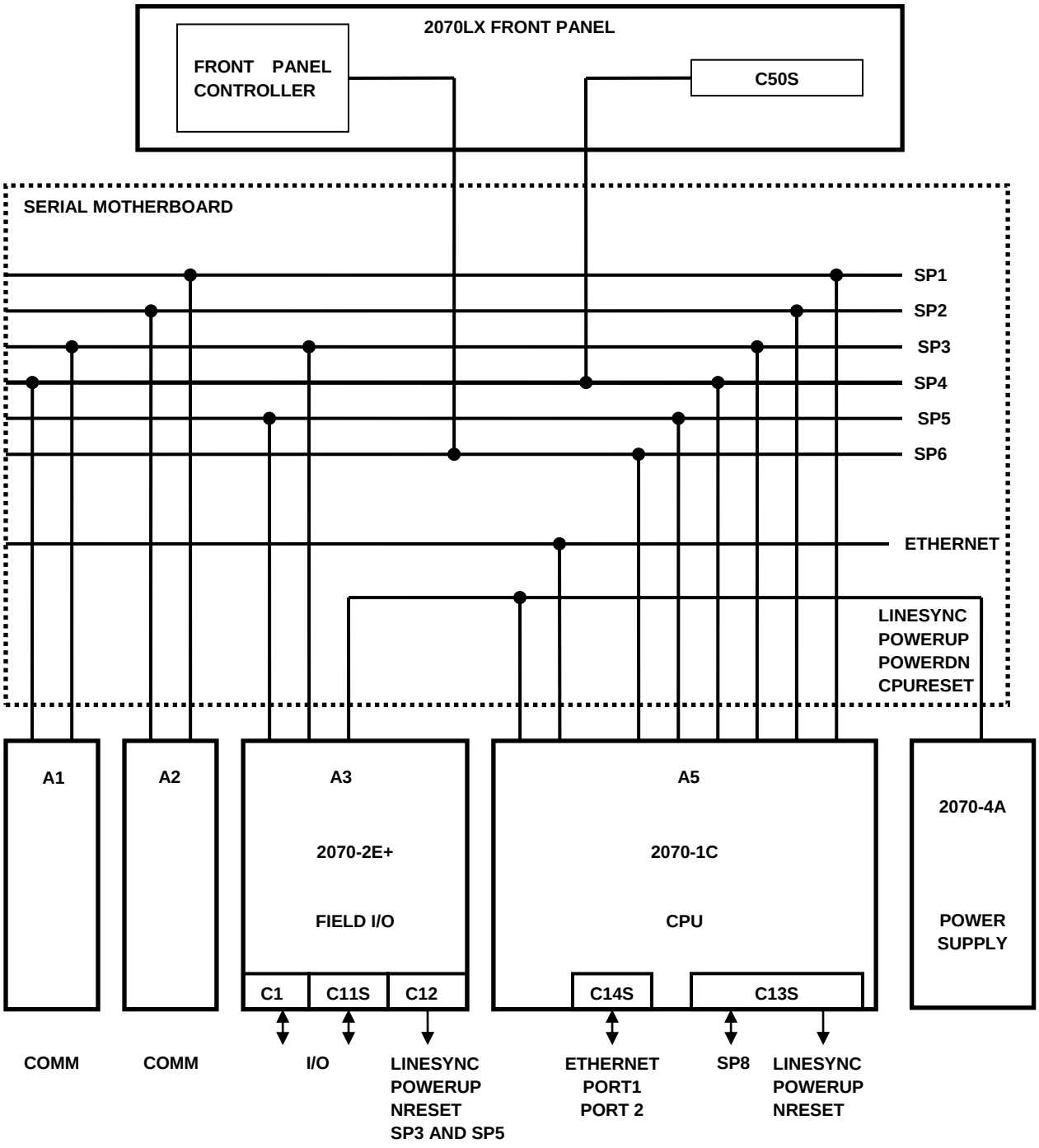


Figure 2: 2070LX Controller System Configuration

1.4 STANDARD FEATURES

Operating system

- Linux, Version 2.6.22

Modules (standard, included)

- 2070-1C CPU Module
- 2070-2E+ Field I/O module
- 2070LX Front Panel Module
- 2070-4A Power Supply

Microprocessors

- MPC8360E Freescale PowerQUICC II Pro microprocessor

Backup real-time clock (RTC)

- Maxim DS1390

Memory

- 256 MB DRAM
- 16 MB Flash Memory NOR
- 256 MB Flash Memory NAND
- 2 MB non-volatile SRAM

Applicable standards

- Meets or exceeds Caltrans TEES 2009 standard

1.5 INTERFACES

Communication interfaces

- Up to five SDLC ports
- Up to seven asynchronous ports
- ENET 1: 100 Base-T Ethernet switch, 1 uplink and 3 additional ports
- ENET 2: 100 Base-T Ethernet port dedicated for local communications (i.e. laptop or similar)
- One USB port

Front panel interface

- Display: 8 lines x 40 characters
- Keyboards: 3 x 4 navigation and 4 x 4 data entry keypads

Cabinet interfaces

- C11S Connector
- C12S Connector
- C1S Connector

2 2070-1C CPU MODULE

2.1 GENERAL DESCRIPTION

The 2070-1C CPU Module is the brain of the controller. It includes the microprocessor computer chip, memory, serial communications and operating system. The 2070-1C is a module meeting the 2X WIDE board requirements. The module is furnished normally resident in the Slot A5 of Motherboard.

The 2070-1C Assembly consists of a Printed Circuit Board Assembly and a front plate. The front plate is attached to the board by using two screws and two washers.

The 2070-1C features a wide variety of communication options, such as serial and Ethernet for connectivity in any kind of environment. Quick data transfers, firmware upgrades, and log retrievals can be done via USB.

The 2070-1C microprocessor is a Freescale MPC8360.

It consists of a Host Board, an Engine Board and a faceplate (plus brackets, standoffs and hardware to fix them to the host board).

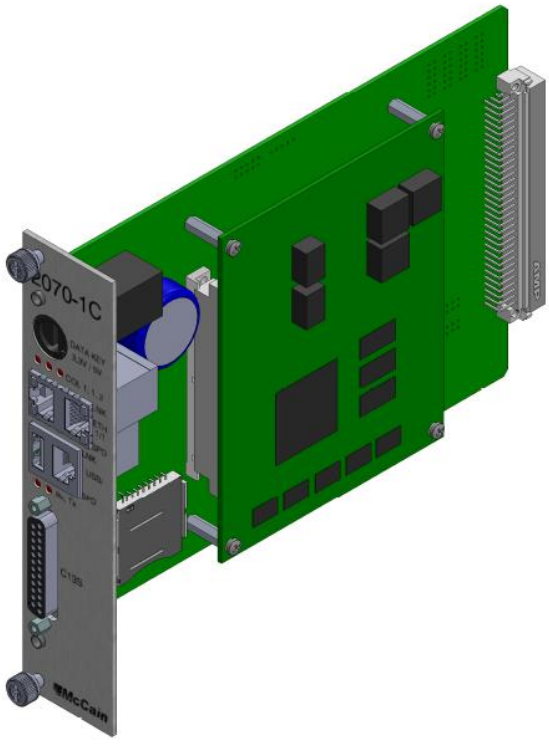


Figure 3: 2070-1C CPU Module

2.2 STANDARD FEATURES

- Operating System: Linux, Version 2.6.22
- Processor: MPC8360E Freescale PowerQUICC II Pro communications processor, 32 Bit, CPU32 Instruction Set.
- Memory:
  - 256 MB DRAM
  - 16 MB Flash Memory NOR
  - 256 MB Flash Memory NAND
  - 2 MB non-volatile SRAM
- Communications:
  - Up to five SDLC ports
  - Up to seven asynchronous ports
  - ENET 1: 100 Base-T Ethernet switch, 1 uplink and 3 additional ports
  - ENET 2: 100 Base-T Ethernet port dedicated for local communications (i.e. laptop or similar)
  - One USB port
- Serial Buses: EIA RS-485 to Motherboard (6 COMM + modem control).
- Time-of-day clock.
- Interrupts.
- CPU Reset.
- CPU activity LED.
- Tick Timer.

2.3 COMMUNICATION INTERFACES' DESCRIPTION

Serial Port 1 (SP-1):

Usage: This is a general purpose port.

Location: available at the DIN-96 connector.

Operating modes: Asynchronous, Synchronous, HDLC, SDLC.

Async rates (bps): 1200, 2400, 4800, 9600, 19.2k, 38.4k / Optional: 57.6k, 115.2k.

Sync rates (bps): 19.2k, 38.4k, 57.6k, 76.8k, and 153.6k.

Interface pins:

SP1_TXD: Transmit Data (O)

SP1_RXD: Receive Data (I)

SP1_RTS: Request To Send (O)

SP1_CTS: Clear To Send (I)

SP1_CD: Carrier Detect (I)

SP1_TXC_INT: Transmit Clock Internal (O)

SP1_TXC_EXT: Transmit Clock External (I)

SP1_RXC_EXT: Receive Clock External (I)

Serial Port 2 (SP-2):

Usage: This is a general purpose port.

Location: available at the DIN-96 connector.

Operating modes: Asynchronous, Synchronous, HDLC, SDLC.

Async rates (bps): 1200, 2400, 4800, 9600, 19.2k, 38.4k / Optional: 57.6k, 115.2k.

Sync rates (bps): 19.2k, 38.4k, 57.6k, 76.8k, and 153.6k.

Interface pins: SP2_TXD: Transmit Data (O)

SP2_RXD: Receive Data (I)

SP2_RTS: Request To Send (O)

SP2_CTS: Clear To Send (I)

SP2_CD: Carrier Detect (I)

SP2_TXC_INT: Transmit Clock Internal (O)

SP2_TXC_EXT: Transmit Clock External (I)

SP2_RXC_EXT: Receive Clock External (I)

Serial Port 3 (SP-3):

Usage: To handle in-cabinet devices.

Location: available at the DIN-96 connector.

Operating modes: Asynchronous, Synchronous, HDLC, SDLC.

Async rates (bps): 1200, 2400, 4800, 9600, 19.2k, 38.4k / Optional: 57.6k, 115.2k.

Sync rates (bps): 153.6k, 115.2k.

Interface pins: SP3_TXD: Transmit Data (O)

SP3_RXD: Receive Data (I)

SP3_RTS: Request To Send (O)

SP3_CTS: Clear To Send (I)

SP3_CD: Carrier Detect (I)

SP3_TXC_INT: Transmit Clock Internal (O)

SP3_TXC_EXT: Transmit Clock External (I)

SP3_RXC_EXT: Receive Clock External (I)

Serial Port 4 (SP-4):

Usage: External user interface and general purpose.

Location: available at the DIN-96 connector.

Operating modes: Asynchronous.

Async rates (bps): 1200, 2400, 4800, 9600, 19.2k, 38.4k / Optional: 57.6k, 115.2k

Interface pins:

SP4_TXD: Transmit Data (O)

SP4_RXD: Receive Data (I)

Serial Port 5 (SP-5):

Usage: To handle in-cabinet devices.

Location: available at the DIN-96 connector.

Operating modes: Synchronous, HDLC, SDLC.

Sync rates (bps): 153.6k, 614.4k.

Interface pins:

SP5_TXD: Transmit Data (O)

SP5_RXD: Receive Data (I)

SP5_TXC_INT: Transmit Clock Internal (O)

SP5_RXC_EXT: Receive Clock External (I)

Serial Port 6 (SP-6):

Usage: Front panel user interface.

Location: available at the DIN-96 connector.

Operating modes: Asynchronous.

Async rates (bps): 1200, 2400, 4800, 9600, 19.2k, 38.4k / Optional: 57.6k, 115.2k

Interface pins:

SP6_TXD: Transmit Data (O)

SP6_RXD: Receive Data (I)

Serial Port 8 (SP-8):

Usage: General purpose.

Location: available at the C13S connector on Front plate.

Operating modes: Asynchronous, Synchronous, HDLC, SDLC.

Async rates (bps): 1200, 2400, 4800, 9600, 19.2k, 38.4k / Optional: 57.6k, 115.2k.

Sync rates (bps): 19.2k, 38.4k, 57.6k, 76.8k and 153.6k.

Interface pins:

SP8_TXD: Transmit Data (O)

SP8_RXD: Receive Data (I)

SP8_RTS: Request To Send (O)

SP8_CTS: Clear To Send (I)

SP8_CD: Carrier Detect (I)

SP8_TXC_INT: Transmit Clock Internal (O)

SPI (Serial Peripheral Interface):

Usage: DATAKEY, EEPROM interface and SD card interface.

Location: DataKey's receptacle at Front plate, serial EEPROM on Host Board and SD card receptacle on the Host board.

Operating modes: Synchronous.

Sync rates (bps): Application specific.

Interface pins:

SPI_MOSI: Master-Out-Slave-In (O)

SPI_MISO: Master-In-Slave-Out (I)

SPI_CLK: Clock (O)

SPI_SEL_1: Select 1 (O)

SPI_SEL_2: Select 2 (O)

SPI_SEL_3: Select 3 (O)

SPI_SEL_4: Select 4 (O)

Universal Serial Bus (USB) Port:

Usage: Facilitate the transfer of data files to/from the CPU by using USB memory devices as an alternative to laptop computer.

Location: One USB connector at Front plate.

Requirements: Hardware and Software conforms to v2.0 USB devices to be used are formatted as

FAT16 file system providing a 2GB storage.

Interface pins:

USB_D+: Data Line Positive (I/O)

USB_D-: Data Line Negative (I/O)

USB_POWER_SWITCH Power Switch (O)

USB_OVERCURRENT Over-current (I)

Ethernet Interface (ENET):

Usage: Local and Network Communications.

Location: Three 10/100BASE-T Ethernet ports on Front plate, ENET1 (2) and ENET2 (1). Four 10/100BASE-T Ethernet ports on the Host board thru 12 pins headers.

Operating modes: Synchronous, Manchester-encoded, and Differential.

Sync rates (bps): 10M, 100M.

Interface pins:

ENET1_TX_POS: Port 1 Transmit Data Positive (O)
ENET1_TX_NEG: Port 1 Transmit Data Negative (O)
ENET1_RX_POS: Port 1 Receive Data Positive (I)
ENET1_RX_NEG: Port 1 Receive Data Negative (I)
ENET2_TX_POS: Port 2 Transmit Data Positive (O)
ENET2_TX_NEG: Port 2 Transmit Data Negative (O)
ENET2_RX_POS: Port 2 Receive Data Positive (I)
ENET2_RX_NEG: Port 2 Receive Data Negative (I)

2.4 THEORY OF OPERATION

The module contains all the circuitry for the CPU function: main processor, FLASH memory, SRAM, RTC, a bidirectional buffer bank for the data, address lines and control lines coming from the processor, the back-up capacitor, RESET circuit, isolation circuit for control signals coming from the power supply, isolation circuit for SP8, C13S connector, Ethernet circuit, DATAKEY circuit, SD card circuit, USB circuit, driver field circuit (RS-485 transceivers), LINESYNC circuit, A2 and A3 connector sensor and A5 connector.

The module is comprised of three main parts: A Host Board, an Engine Board and a Faceplate.

The faceplate is a 2X wide aluminum front plate with the necessary cutouts for the front connections; it also has thumbscrews to be attached to the chassis.

2.4.1 Host board

This board provides the mechanical and electrical interface to the Engine Board. All circuitry related to the power, communications, control, status, and signal conditioning to be provided to the Engine board is done here.

The board includes: DIN-96 connector, C13S Connector circuitry, control signals circuitry (Power Down, Power Up, Linesync and CPU Reset), receptacles for engine board installation, voltage regulators, RS-485 line driver/receiver circuitry, backup circuitry, Ethernet switch, USB, Datakey circuitry, SD card receptacle, ACTIVE LED circuitry, A2-A3 installation detection circuitry, ESD protection, etc.

2.4.1.1 The DIN-96 Connector

The 96-pin DIN connector is the physical interface between the CPU and the serial motherboard A5 slot.

It carries the RS-485 differential signals for the serial communication ports SP-1, SP-2, SP-3, SP-4, SP-5 and SP-6; the Ethernet port lines, A2 and A3 install lines, FPALED line, CPURESET line, and the interruption signals LINESYNC, POWERUP and POWERDOWN.

2.4.1.2 C13S Connector circuitry

C13S Connector is a 25-positions D-sub connector that is used to support the serial communication port SP-8 and the control lines (Linesync, Reset, Power Down).

It consists of RS-485 drivers and receivers, opto-isolators and inverter gates.

SP-8 single ended transmission signals TxCLKO, RTS and TxD coming from the Engine Board (Connector P2) are inverted, isolated, converted to differential line signals at the differential line driver and then routed to the C13S connector.

SP-8 differential line signals RxCLK+, RxCLK-, RxD+, RxD-, CTS+, CTS-, DCD+, DCD-, received at the C13S connector are converted to single ended signals at the differential line receiver, isolated and then routed to the Engine Board through the connector P2.

The +5VDC isolated power supply is achieved by using the incoming +12VDC ISO from 2070 power supply, a +5VDC voltage regulator and two capacitors.

This isolated supply is used to power the isolation circuitry and RS-485 circuitry for SP-8 communication signals and external interrupts, also as an isolated supply at C13S connector.

2.4.1.3 Control signals circuit

LINESYNC, POWERUP and POWERDN are the external interruption signals used to generate internal CPU's control signals.

These signals are generated at the 2070-4A module power supply, routed to the Serial Motherboard and received through the A5 connector.

Once received these signals are routed to the Engine Board through the P2 connector. Also, these signals are inverted, isolated (POWERUP is ORed with CPULRESET at this stage to generate the RESET signal), converted to differential line signals and then routed to C13S connector.

2.4.1.4 Receptacles for engine board installation

P1 and P2 are the two 50-position receptacle connectors that provide an interface between the Engine board and Host board, they carry the RS-485 differential signals for the serial communication ports SP-1, SP-2, SP-3, SP-4, SP-5, SP-6, and SP-8; for the SPI bus, also the CPU_ACTIVE LED, Ethernet, DATAKEY and USB lines, +5VSTANDBY and interruption signals LINESYNC, POWERUP and POWERDOWN.

2.4.1.5 RS-485 line driver/receivers circuitry

The RS-485 line driver/receiver circuitry is the interface for the serial communication ports between the serial motherboard and the Engine Board. This stage converts the RS-485 differential signals provided by the serial motherboard at A5 connector to a single ended signal to be used by the Engine Board. This circuitry also receives the single ended signals from the Engine Board and converts them to RS-485 differential signals to be sent to the serial motherboard. Some enabling/disabling control for the receivers and drivers is added at this stage.

Receivers:

The differential signals coming from the serial motherboard through A5 enter to the line receivers to be converted into single ended signals and then routed to the Engine Board through the P1/P2 connectors.

Five quadruple differential line receivers SN65LBC173A are used to receive the serial communication differential signals of SP-1, SP-2, SP-3, SP-4, SP-5 and SP-6 ports. The two enable inputs of the line receiver are accordingly tied to +5VDC and GND, permanently enabling all receivers, then the reception of serial communications is always enabled.

Reception signals:

SP-1: RxD+, RxD-, CTS+, CTS-, TxCLKI+, TxCLKI-, RxCLK+, RxCLK-, DCD+, DCD-.

SP-2: RxD+, RxD-, CTS+, CTS-, TxCLKI+, TxCLKI-, RxCLK+, RxCLK-, DCD+, DCD-.

SP-3: RxD+, RxD-, CTS+, CTS-, TxCLKI+, TxCLKI-, RxCLK+, RxCLK-, DCD+, DCD-.

SP-4: RxD+, RxD-.

SP-5: RxD+, RxD-, RxCLK+, RxCLK-.

SP-6: RxD+, RxD-.

Drivers:

The single ended signals coming from the Engine Board through the P1/P2 connectors enter to the line drivers to be converted into differential signals and then routed to the A5 connector on serial motherboard.

Four quadruple differential line drivers SN65LBC174A are used to transmit the communication differential signals of SP-1, SP-2, SP-3, SP-4, SP-5 and SP-6 ports.

SP-1 and SP-2 transmission is enabled by the line A2_INSTALL; when this line is LOW the drivers are disabled, when HIGH the drivers are enabled.

SP-3 transmission is permanently enabled (enable input is tied to +5VDC) on the drivers.

SP-5 transmission is enabled by the line A3_INSTALL; when this line is LOW the drivers are disabled, when HIGH the drivers are enabled.

SP-4 and SP-6 transmission is permanently enabled on the drivers (enable inputs are tied to +5VDC).

Transmission signals:

SP-1: TxD+, TxD-, TxCLKO+, TxCLKO-, RTS+, RTS-.

SP-2: TxD+, TxD-, TxCLKO+, TxCLKO-, RTS+, RTS-.

SP-3: TxD+, TxD-, TxCLKO+, TxCLKO-, RTS+, RTS-.

SP-4: TxD+, TxD-.

SP-5: TxD+, TxD-, TxCLK+, TxCLK-.

SP-6: TxD+, TxD-.

2.4.1.6 Back up circuitry

This circuit provides a proper backup power source to the Engine Board in order to keep the required functions working properly, i.e.: RTC and SRAM data.

It consists of a 2.2F 5VDC super capacitor, two common cathode dual diodes and a 150 ohm series resistor.

This circuit is fed by the on-board +5VDC and the +5VDC standby from Power Supply, theses voltages feed the super capacitor through a common cathode dual diode and a current limiting series resistor, the super capacitor then delivers the standby voltage to the Engine Board through the other common cathode dual diode.

2.4.1.7 Ethernet switches

The Host Board provides two, Layer 2, managed switches with auto-switching capability for both 10BASE-T and 100BASE-T systems.

Each switch provides five Ethernet transceivers; all PHY units support 10BASE-T and 100BASE-TX. In addition, two of the PHY units support 100BASE-FX (port 4 and port 5).

Each switch is connected to an independent Ethernet port coming from the Engine Board called ENET1 and ENET2.

The Ethernet ports distribution on the Host Board is as follow:

ENET1 Port 0: This port is connected to the Engine Board's ENET1 port.

ENET1 Port 1: This port is provided through an RJ-45 Ethernet connector on the CPU's front plate.

ENET1 Port 2: This port is provided through an RJ-45 Ethernet connector on the CPU's front plate.

ENET1 Port 3: This port is provided through a 12 pins header designated as "CONN1" on the host's PCB.

ENET1 Port 4: This port is provided through the A5 bus to the serial motherboard.

ENET2 Port 0: This port is connected to the Engine's board ENET2 port.

ENET2 Port 1: This port is provided through an RJ-45 Ethernet connector on the CPU's front plate.

ENET2 Port 2: This port is provided through a 12 pins header designated as "CONN2" on the host's PCB.

ENET2 Port 3: This port is provided through a 12 pins header designated as "CONN3" on the host's PCB.

ENET2 Port 4: This port is provided through a 12 pins header designated as "CONN4" on the host's PCB.

All Ethernet ports are magnetically isolated from internal or field connections via isolation transformers with the proper characteristic impedance.

The Ethernet switches are configured via an EEPROM. Also, they can be configured via a 10-positions header.

2.4.1.8 USB Hub

The USB Hub expands the USB host port coming from the Engine Board by repeating the bus in order to increase the number of ports available and thus allow two devices to be connected to the host port.

The USB hub provides one upstream port and four downstream ports. The upstream port connects the hub directly to the host port on Engine Board and the downstream ports are routed to the USB receptacle and USB header connectors on the Host board.

The circuitry is comprised of the USB hub controller, a 24MHz oscillator, common mode chokes, dual supervisory power control switches for all ports and one USB receptacle.

The Host Board provides a USB 2.0 hub controller with integrated upstream and downstream transceivers, a USB Serial Interface Engine (SIE), USB Hub Control and Repeater logic, and Transaction Translator (TT) logic.

The 3.0VDC/5VDC dual supervisory power control switches supply 500mA minimum and limit fault currents to 2A, the flag output pin for each switch is available to indicate fault conditions to the USB controller. The soft start feature eliminates a momentary voltage drop on the upstream port that may occur when the switch is enabled in bus-powered applications. The thermal shutdown feature prevents damage to the device when subjected to excessive current loads. The under voltage lockout feature ensures that the device remain off unless there is a valid input voltage present. There are three dual supervisory power control switches on the Host Board, one for supplying power to the USB host controller and one for supplying power to each port on the USB receptacles.

Common mode chokes are suited for common mode noise suppression on the USB lines because of the large current flow. The USB host port from the Engine Board enters to the hub controller through common mode chokes and also the downstream ports enter to the USB receptacles and connection headers through common mode chokes.

2.4.1.9 Datakey circuitry

This circuit consists of a serial memory key receptacle which contains a Last-On/First-OF (LOFO) switch that ensures the key does a secure contact before any signal is transmitted and support circuitry for interfacing it with the processor.

It is implemented by using a DATAKEY receptacle KC4210PCB, three buffer gates and one PNP transistor.

For any Data Key operation the data key driver samples the LOFO line, if the line is cleared (logic low 0VDC) the driver powers up the data key to begin the requested operation. After the operation is finished the data key is powered down until another operation is requested.

Once the data key has been detected and energized by the LOFO switch, the driver tries to communicate using the I2C protocol to get the drive ID and memory size, if there is no response, it tries again with the SPI protocol if this also results in a no response situation then all communication with the data key is halted until a new operation is requested (an error code will be generated when this event occurs). After a response is successfully obtained from the data key the requested operation will begin. If any error is detected during the operation, an error code will be returned and communications will be halted.

2.4.1.10 ACTIVE LED circuit

This circuit is activated/deactivated by the CPU_ACTIVE signal coming from Engine Board and generates a control signal that goes to the Serial Motherboard and then to the Front Panel Assembly for controlling the ACTIVE LED's status.

This circuit is comprised of a NPN transistor, a limiting resistor for base current and a pull-up resistor connected to +5VDC at the collector. The FPALED signal is at +5VDC while the transistor is deactivated and at logic ground when activated.

2.4.1.11 A2-A3 installation detection circuitry

This circuit is used to let the CPU know when the A2 and/or A3 slots on serial motherboard have installed a 2070 type card.

The circuitry consists of two inverter gates with the inputs to a pull-up and connected to the sensing lines on A5 connector, these two lines come from the A2 and A3 slot connectors on serial motherboard. The output of the inverter gates is LOW until A2 and/or A3 are used.

A2 INSTALL: When A2 slot on serial motherboard is used, this line drives to GND forcing the output of the inverter gate to HIGH. This line enables the corresponding differential line drivers for SP-1 and SP-2 transmission.

A3 INSTALL: When A3 slot on serial motherboard is used, this line drives to GND forcing the output of the inverter gate to HIGH. This line enables the corresponding differential line drivers for SP-5 transmission.

2.4.1.12 SD CARD Circuit

It is implemented by a SD Card push in, push out connector, two quadruple bus buffer gate, resistors and a PNP Transistor BC807. This circuit it is controlled by four lines: CS_SDCARD, SPI_CLK, SPI_MOSI and SPI_MISO. The CS_SDCARD line is used to select and deselect the chip, the SPI_CLK line it is generated by the master and it is the clock signal, the SPI_MOSI it is the data signal generated by the master which it is read by the slave, in this case the SD Card and the SPI_MISO line it is the data signal generates by the slave and which is read by the master.

2.4.2 Engine Board

The Engine Board is the brain of the 2070LX controller; all computational functions are concentrated on this board. It is comprised of basically four sub-systems: Processor, Memory, Communications and Reset management. These sub-systems are comprised of the Processor and some interfaces and support circuitry.

The engine provides two 50-position interface connectors and four standoff holes to allow the installation onto a Host Board. Four 4-40 hex threaded standoffs are used between the modules and 4-40 mating screws to fix them together.

Below are the sub-systems with a little explanation about how they are comprised and the intended functionality.

2.4.2.1 Microprocessor

The PowerQUICC II Pro Processor MPC8360 takes care of all operations and processes performed on the Engine board:

- It runs the application software.
- Administers the address, data and control buses for communicating to memories and other peripheral devices.
- Manages read/write memory operations for storage and data collection.
- Controls the communications: Seven serial ports, two Ethernet ports, one USB port, one SPI bus, one local I2C bus, one BDM bus.
- Monitors and sets the status of important input/output signals (Powerup, Powerdown, Linesync, Datakey present, CPU Active, CPU Reset, etc).

2.4.2.2 Memory

NAND flash memory

The Engine Board has a NAND Flash Memory configured as 256 MB. This device use a highly multiplexed 8-bit bus to transfer commands, address and data and it is designed to prevent data corruption during power transitions.

NOR flash memory bank 4M x 16 x 2

The Engine Board has two bank of Parallel NOR Flash Embedded Memory which are configured as 4M x 16bit, the Flash Memory is a 64 Mbit nonvolatile memory that can be read, erased and reprogrammed. The total NOR flash on the Engine Board is 16 MB.

SRAM 1M x 16

This 16M memory (SRAM), 1M X 16bit, is used to store all of the non-volatile data, it has a battery back-up in order to avoid losing data during a power failure on AC line. The total SRAM on the Engine Board is 2 MB.

DDR bank memory 64M x 64

The Engine Board has five DDR2 SDRAM which uses a double data rate architecture to achieve high-speed operation. The DDR2 SDRAM is a high-speed CMOS, dynamic random access memory, it is internally configured as a multibank DRAM and operates from a differential clock.

Read and write accesses to the DDR2 SDRAM are burst-oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVATE command, which is the followed by a READ or WRITE command.

RTC

The RTC circuit in the Engine Board it is implemented by a low-voltage serial-peripheral interface (SPI) real-time clock with trickle charger DS1390 and a 32.768k external quartz crystal.

The real time clock is a software-settable clock and calendar device with a 100ms resolution. It is connected to Vcc and to the standby voltage supply and provides information to the processor through the SPI bus.
The time is provided to the controller at boot time, and then the controller updates the RTC time every hour.
It monitors the status of Vcc and if a power failure is detected, it automatically disables the bus interface and switches to the backup supply maintaining the accuracy requirements. Once the power is reapplied the RTC is used to set the time/date of the OS.

2.4.2.3 Communications

The PowerQUICC II Pro Processor MPC8360 takes care of all communications on the Engine Board.

- Seven serial ports called SP-1, SP-2, SP-3, SP-4, SP-5, SP-6 and SP-8.
- Two Ethernet ports ENET1 and ENET2.

- One USB port.
- One SPI bus for interacting to the Datakey and SD card on Host Board and the RTC on Engine Board.
- One local I2C bus for interfacing to the Boot EEPROM.
- One BDM bus for allowing the programming.
- Monitors and sets the status of important input/output signals (Powerup, Powerdown, Linesync, Datakey present, CPU Active, CPU Reset, etc).

2.4.2.4 Reset management

The Engine Board provides an active-low, +5VDC, output signal called CPU_RESET. It is used to reset other internal/external system devices.

This output signal is generated by the CPU Reset line circuit. This circuit acts as an OR gate that receives two input signals, both are provided by the Processor, one input signal is related to a hardware reset and the other one to a software reset.

- Hardware Reset

  This active-low reset signal is provided by the Processor upon the process of an input signal representing a reset condition. This reset condition is the output of a two inputs AND gate, one input signals is POWERUP and the other one is an output from a supervisory circuit.

  POWERUP is an active-low Power Supply's control signal triggered by a long power outage.

  The active-low output signal from the supervisory circuit is caused by a low-voltage condition at Vcc.

- Software Reset

  This active-low reset signal is provided by the Processor upon the process of a reset command from the application software.

2.4.2.5 Support circuitry

In order for the main sub-systems to operate on the Engine Board, there is support circuitry related to the functionality such as connectors, buffers, drivers, USB and Ethernet transceivers, programming test ports, Linesync and ACFail control circuit, Reset circuits, microprocessor supervisory circuit, backup circuit, memory & peripherals' power source and CPU's core power source.

Also there are some special signals related to monitoring, status and control.

50-position Connector Headers

P1 and P2 are two 50-position double row connector headers that are used; they are located properly in order to be plugged into any Host board meeting this standard.

It has all the necessary connections from all circuitry on Engine board so that they have their corresponding lines on the Host board.

Octal buffers/drivers

These LV541A devices are used for driving the communication, status and control lines between the processor on engine board and the related circuitry on Host Board; these lines are SP-1 to SP-8, SPI bus, CPULRESET, CPUACTIVE, POWERUP, DATAKEY present and USB signals.

These devices are used as voltage level translators because their inputs can be driven at either 5VDC or 3.3VDC allowing them to work in a mixed 3.3VDC/5VDC system environment.

The devices are permanently enabled; the 3-state control gates (OE1 or OE2) are tied to ground.

There are two types of buffer/drivers used:

LV541AP are used to “translate” the 5VDC level from Host Board signals to 3.3VDC level to be used on Engine Board.

LV541AT are used to “translate” the 3VDC level from Engine Board signals to 5VDC level to be used on Host Board.

Octal bus transceivers

These devices provide a data bus interface between the Processor and the memories (SRAM, FLASH).

They transmit data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control input (DIR).

Processor writes data to memory by setting a high logic level at the DIR input; it reads data from memory by setting a low logic level at the DIR input.

The output-enable (OE) is tied to ground so that the devices are permanently enabled.

USB transceiver

The USB transceiver interfaces the standard logic to the physical layer of the Universal Serial Bus. This means that the Processor is in charge of the USB logic functionality and the transceiver is responsible of the compliance, signal integrity and signal quality issues related to driving and receiving differential signals.

Features:

- The transceiver converts USB differential voltages to digital logic signal levels.

It converts the D+ and the D- line to single ended logic outputs.

- It converts logic levels to different USB signals: it runs at low or high speed, it has selectable output slope control, it meets the USB 1.1 drive template, it has low power standby mode.

The transceiver provides a differential I/O data bus (D+ and D-) for communications with the Host Board.

It has two inputs for receiving all data from the Processor and two logic-level outputs (buffered version of D+ and D-) to the Processor. It also provides an output from the USB differential input that goes into the Processor.

There is an active-low input that enables the transceiver to transmit data on the bus; when disabled it is in receive mode.

An active-high input tied to 3.3VDC enables the transceiver to enter to a low-power state while USB is inactive.

10Base-T / 100BASE-TX/FX Ethernet ports

There are two Ethernet ports on the Engine Board and each port has a unique 48-bit MAC address.

Each Ethernet port consist of the Processor's Ethernet Controller, an Ethernet transceiver, a 25MHz crystal, status LED's, a magnetic transformer and different resistors and capacitors for setting the configuration.

The KS8721 transceiver's purpose is physical; it implements the hardware functions for sending and receiving the Ethernet frames; it handles the line modulation at one side and the binary packet signaling at the other side.

The interface consists of data signals, management signals and an interrupt signal to alert the Processor of status change at the physical layer. MII (Media Independent Interface) is set by default mode after power-up. The MII bus transfers data using 4-bit words (nibble) in each direction (4 transmit data bits, 4 receive data bits). The data is clocked at 25 MHz to achieve 100 Mbit/s speed. The transceiver automatically configures themselves for 100 or 10Mbps and full or half-duplex operation, using an on-chip auto-negotiation algorithm. It also has on-chip 10BASE-T output filtering, eliminating the need for external filters and allowing a single set of line magnetics to be used to meet requirements for both 100BASE-TX and 10BASE-T.

Programming/Test port

There is a 16-position connector header on Engine Board and it is used as a manufacturer-specific BDM interface port for programming and test on-board devices.

Linesync and ACFail Control circuit

This circuit receives the Linesync and ACFail signals from the Power Supply and buffers them for the Processor.

The circuitry consists of a "D" type flip-flop, an inverter gate and three buffer gates.

2.4.2.6 Reset Circuits

Microprocessor supervisory circuit MAX795

This microprocessor supervisory circuit monitors and controls the activities of the Processor. One feature is µP reset. The threshold voltage range is from 3VDC to 3.15VDC. Its reset signal is an open-drain, active-low output that drives low for 200ms when triggered and stays low while Vcc is below the threshold. Once Vcc rises above the threshold level, the output remains low for 200ms.

Power On Reset Circuit / Hardware Reset Circuit

This circuit consists of one AND gate and two input signals; it receives the POWERUP signal and the reset signal from the MAX795, if any of the signals is asserted, the gate generates an active-low reset signal that goes to the FLASH memories and to the Processor. The Processor, based on the status of this signal generates a hardware reset that results in a CPULRESET.

POWERUP: This signal comes from the Power Supply. It is a status signal that indicates whether the AC power requirements are met. It is high while the requirements are met, otherwise it is low.

MAX795 Reset: This signal comes from the microprocessor supervisory circuit.

CPULRESET Line circuit

The CPULRESET is an active-low, +5VDC output signal provided by the Engine board in order to reset other devices.

This signal is generated by the CPU RESET Line circuit and responds to two input signals provided by the Processor, CPURESET and /RSTO.

CPURESET line is asserted when the application program receives a reset command or when /RSTO line is asserted when the Processor receives a Power On Reset/Hardware reset.

The circuitry consists of two N-Channel MOSFET's with the Drain connected to the same pull-up resistor and the Source connected to logic ground. The CPURESET line controls one MOSFET and the other MOSFET is controlled by an inverter gate that receives /RSTO as an input.

This circuit acts as an OR gate. If any of the two lines are asserted, the CPURESET line is also asserted by being pulled to logic ground. The CPU Reset line then goes through a buffer to convert it to a 5VDC signal and then goes to the P2 connector.

Microprocessor supervisory circuit with SRAM backup

The MAX795 microprocessor supervisory circuit monitors and controls the activities of the Processor by providing some features such as: Processor reset, write protection for the SRAM and backup switchover.

Processor reset

This device has a reset threshold voltage range of 3.00VDC to 3.15VDC. The open-drain, active-low, reset output goes low for 200ms when triggered and stays low while the voltage supply is below the threshold. Once the voltage supply rises above the threshold level the output remains low for 200ms.

The SRAM write protection

This circuitry prevents writing to the SRAM and keeps the processor in a RESET state while the voltage supply is not within specification; POWERUP and POWERDOWN signals are not taken into account.

This circuit has its chip-enable input connected to the Processor and its chip-enable output to the SRAM. The chip-enable output goes low only when chip-enable input is low and reset is not asserted.

If chip-enable input is low when a reset occurs, the chip-enable output remains low for 10µs or until the chip-enable input goes high, whichever occurs first.

Backup switchover

This device provides the supply output for the SRAM; when the voltage supply is above the reset threshold or backup, the supply output is connected to the voltage supply, otherwise it is connected to the backup.

- **Backup circuit**

  This circuit receives the backup voltage a super capacitor located on Host Board, reduces its level and feeds the microprocessor supervisory circuit and the RTC with a proper backup voltage.

  It consists of a series resistor to limit the current consumption and four zener diodes to limit the voltage to +3.3VDC.

CPU's core power source

The CPU's power source is based on the LM3743MM-300 High-Performance Synchronous Buck controller in a typical application.

This DC/DC voltage mode PWM buck controller features synchronous rectification at 300 kHz. It delivers current as needed and step down from an input voltage of +5VDC down to a voltage of +1.2VDC. This voltage is then fed to the CPU's core.

The LM3743 provides a set of comprehensive fault protection features such as high-side current limit, output under-voltage protection, and low-side current limit; if any of these fault protection features is engaged, it enters into "hiccup" protection. It also ensures a smooth and controlled start-up supporting pre-biased outputs.

Memory and peripherals' power source

The Memory and peripherals' power source is based on the LM5642X Dual Synchronous Buck Converter in a typical two channel application circuit.

This converter consists of two current mode synchronous buck regulator controllers operating 180° out of phase with each other at a normal switching frequency of 375 kHz. Out of phase operation reduces the input RMS ripple current, thereby significantly reducing the required input capacitance.

The two switching regulator outputs are independently adjusted:

One regulator is adjusted to 1.8VDC @ 7A for providing power to the DDR2 memory.

The other regulator is adjusted to 3.3VDC @ 4A in order to provide power for almost all circuitry on Engine Board: Boot EEPROM, SRAM and FLASH memories, CPU, uP supervisory circuit, RTC, USB transceiver, buffer, drivers, transceivers, transparent latches, logic gates, Linesync & ACFail control circuit, CPULRESET line circuit, etc; except the two Ethernet transceivers.

Over-voltage protection is available for both outputs. Its current-mode feedback control assures excellent line and load regulation and wide loop bandwidth for excellent response to fast load transients. It also features analog soft-start circuitry that is independent of the output load and output capacitance making the soft-start behavior more predictable and controllable.

Power Interruption, Power Restoration and Synchronization signals

POWERDOWN
This is a +5VDC input signal to the Engine Board. During normal operation it is at high state; During AC power failures it goes to low state; if it is a short power outage, there is no reset and the application software continues operating normally. If it is a long power outage then a reset is performed.

POWERUP
It is a +5VDC input signal to the Engine Board. During normal operation it is at high state; during a long power outage it drives to low state causing all software execution to be halted, once power is restored a cold restart is performed.

LINESYNC
The LINESYNC signal is a +5VDC signal input to the Engine Board. It provides a 50% duty cycle square-wave at 60Hz and it is used provide a periodic interrupt to the Processor as a clock reference.

Miscellaneous signals

CPU_ACTIVE
This is an active-low, +5VDC output signal provided to indicate an active CPU and is accessible to application programs. The typical use for this signal is to drive a front-panel's 'ACTIVE' LED.

DKEY_PRESENT
This is an active-low, +5VDC input signal to the Engine Board. When this signal is active, it indicates the physical presence of a secured key in the DataKey receptacle.

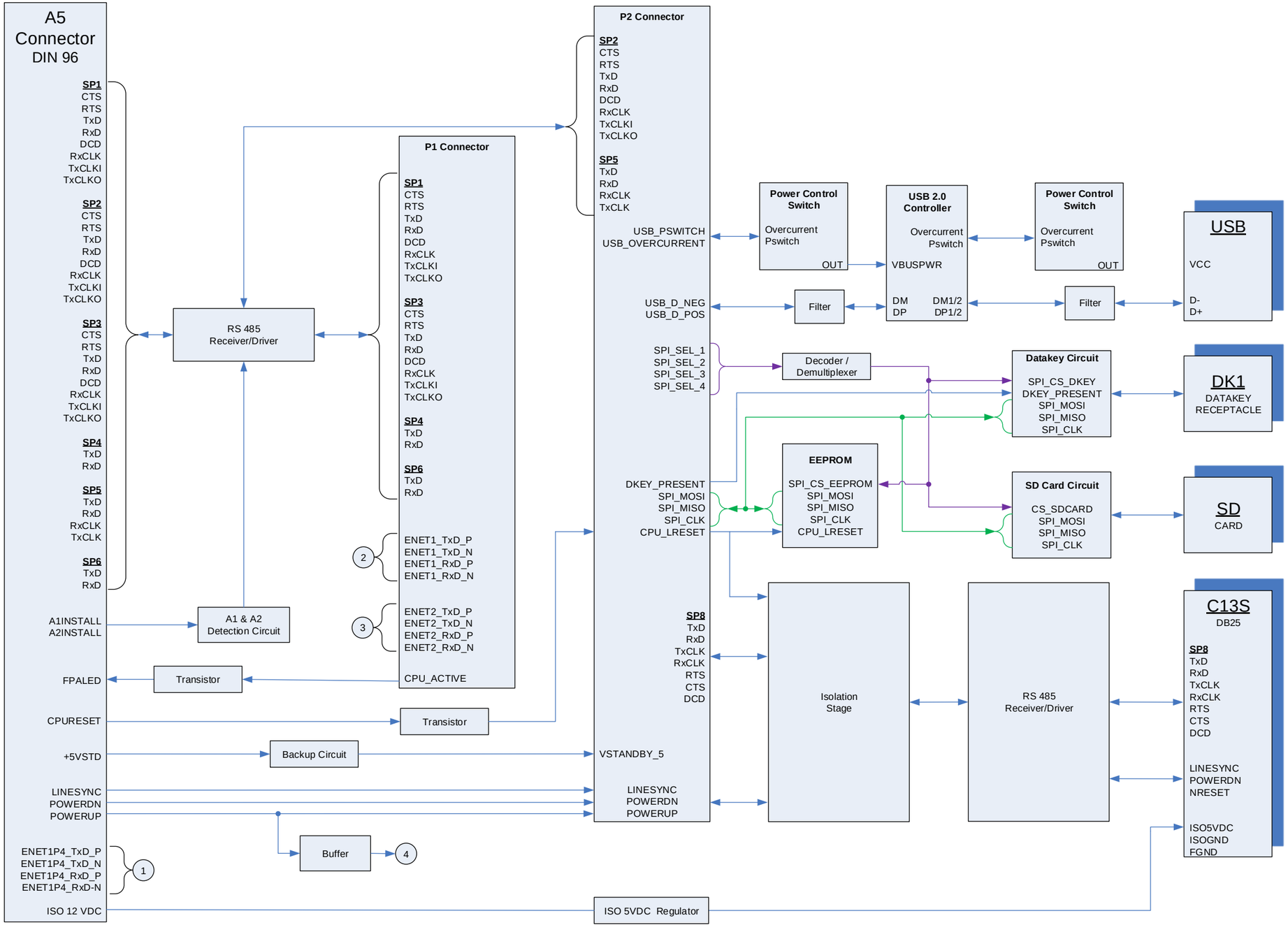
ENGINE_PRESENT
This is an active-low output signal from the Engine Board; it is physically connected to logic ground. It indicates the physical presence of an Engine Board to the Host Board.

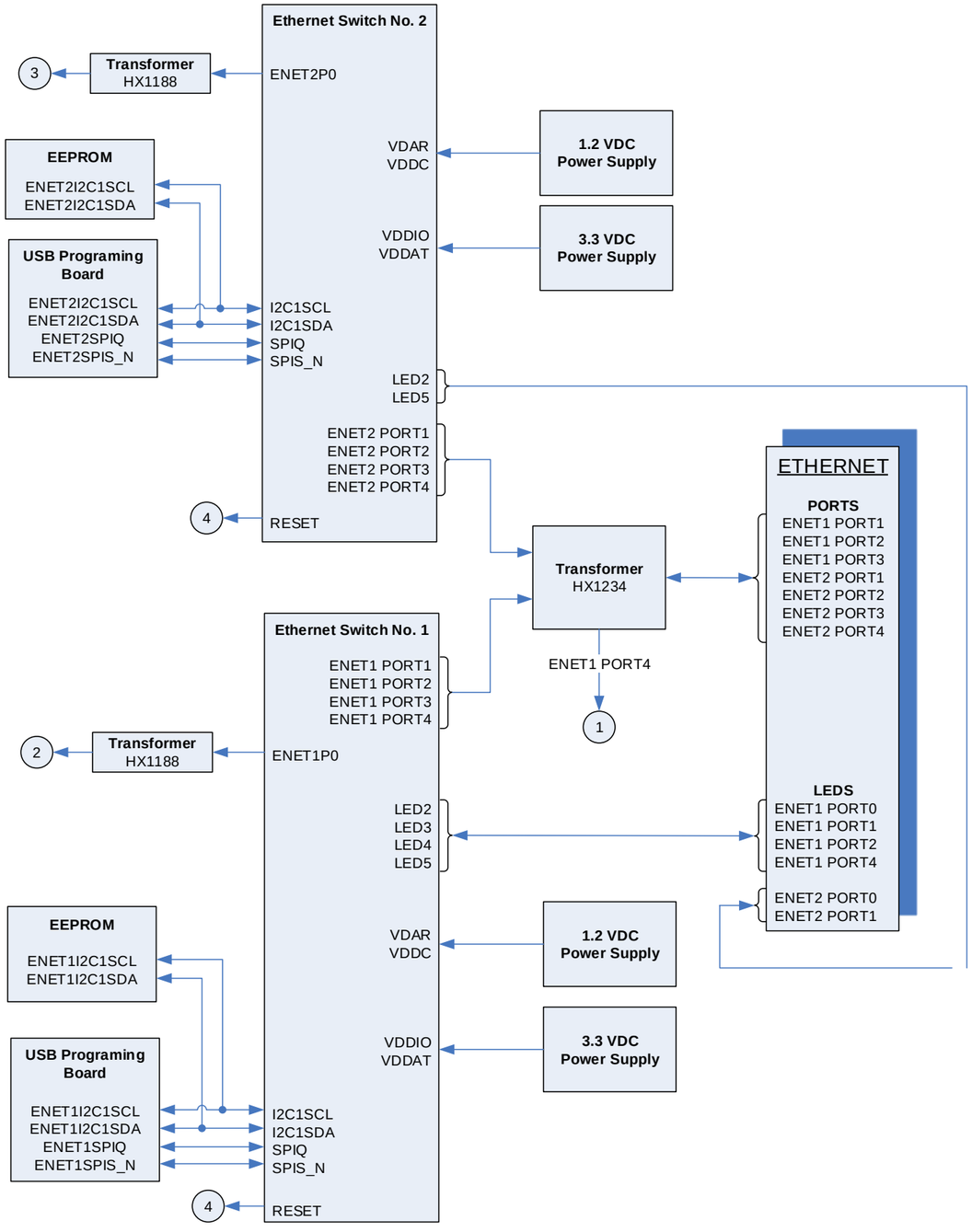
EQUIPMENT GROUND
The Equipment Ground is routed from Host Board to Engine Board through a mounting hole located near to pin 50 at P1 connector.

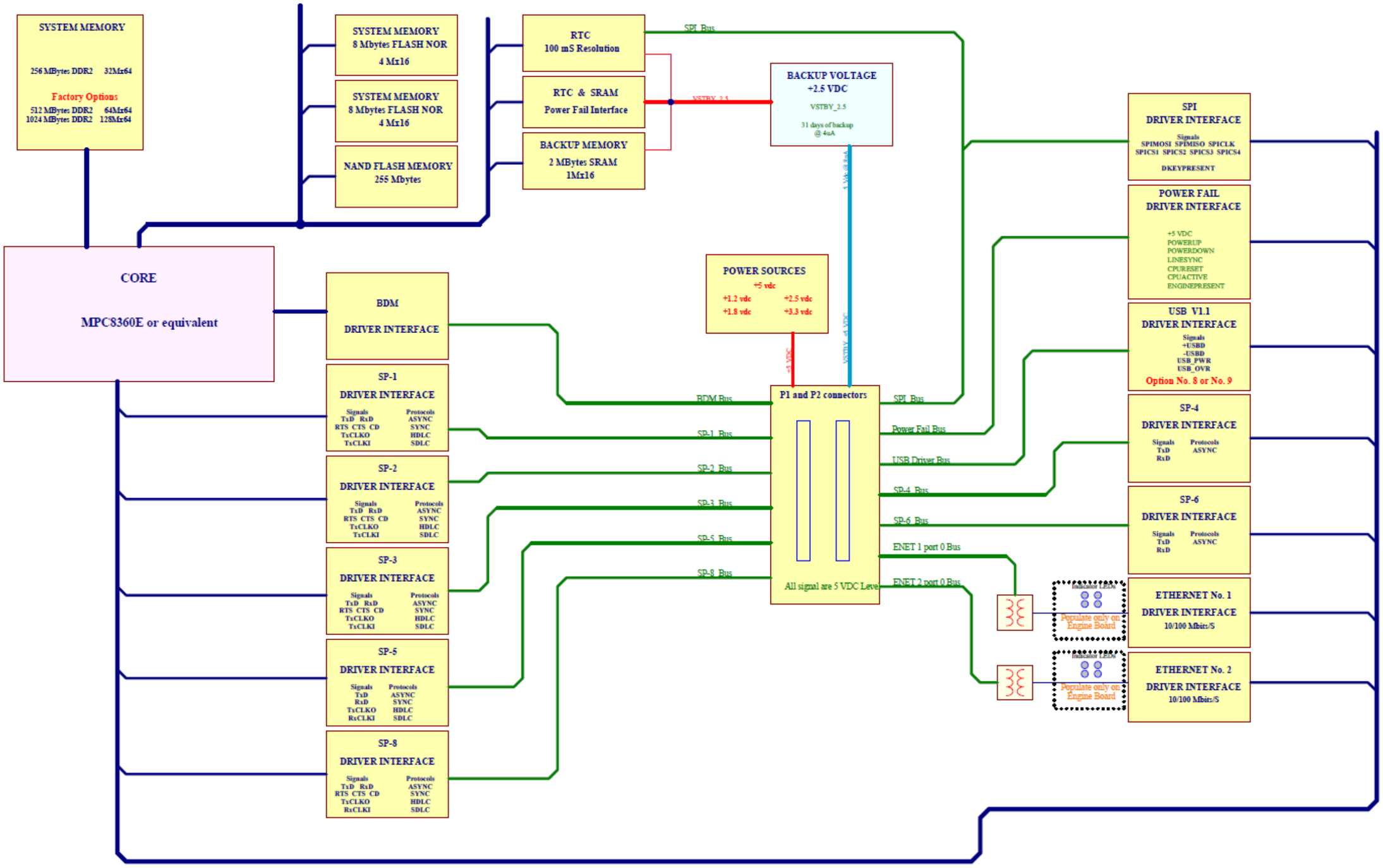
RESERVED

There are some pins at the 50-position connectors on both Engine Board and Host Board that are not used; in accordance with the 5.2b specification these pins are reserved for future enhancements.

2.5 2070LX HOSTBOARD AND ENGINE BLOCK DIAGRAMS




Ethernet Switch No. 2
3
Transformer
HX1188
ENET2P0
EEPROM
ENET2I2C1SCL
ENET2I2C1SDA
USB Programing Board
ENET2I2C1SCL
ENET2I2C1SDA
ENET2SPIQ
ENET2SPIS_N
VDAR
VDDC
1.2 VDC Power Supply
VDDIO
VDDAT
3.3 VDC Power Supply
I2C1SCL
I2C1SDA
SPIQ
SPIS_N
LED2
LED5
ENET2 PORT1
ENET2 PORT2
ENET2 PORT3
ENET2 PORT4
4
RESET
Transformer
HX1234
ETHERNET
PORTS
ENET1 PORT1
ENET1 PORT2
ENET1 PORT3
ENET2 PORT1
ENET2 PORT2
ENET2 PORT3
ENET2 PORT4
Ethernet Switch No. 1
ENET1 PORT1
ENET1 PORT2
ENET1 PORT3
ENET1 PORT4
ENET1 PORT4
1
2
Transformer
HX1188
ENET1P0
LED2
LED3
LED4
LED5
LEDS
ENET1 PORT0
ENET1 PORT1
ENET1 PORT2
ENET1 PORT4
ENET2 PORT0
ENET2 PORT1
EEPROM
ENET1I2C1SCL
ENET1I2C1SDA
VDAR
VDDC
1.2 VDC Power Supply
USB Programing Board
ENET1I2C1SCL
ENET1I2C1SDA
ENET1SPIQ
ENET1SPIS_N
VDDIO
VDDAT
3.3 VDC Power Supply
I2C1SCL
I2C1SDA
SPIQ
SPIS_N
4
RESET

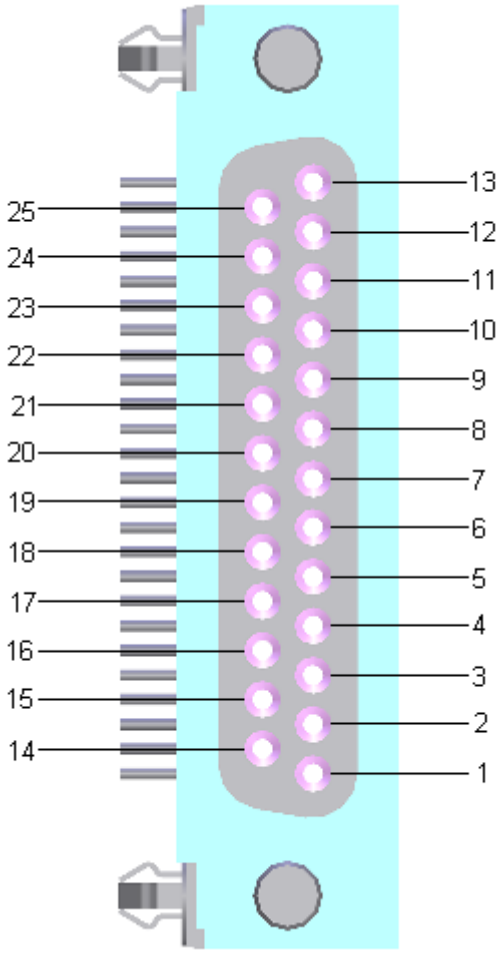

SYSTEM MEMORY
256 MBytes DDR2 32Mx64
Factory Options
512 MBytes DDR2 64Mx64
1024 MBytes DDR2 128Mx64
SYSTEM MEMORY
8 Mbytes FLASH NOR
4 Mx16
SYSTEM MEMORY
8 Mbytes FLASH NOR
4 Mx16
NAND FLASH MEMORY
255 Mbytes
RTC
100 mS Resolution
RTC & SRAM
Power Fail Interface
BACKUP MEMORY
2 MBytes SRAM
1Mx16
SPI Bus
VSTBY_2.5
BACKUP VOLTAGE
+2.5 VDC
VSTBY_2.5
31 days of backup
@ 4uA
CORE
MPC8360E or equivalent
BDM
DRIVER INTERFACE
POWER SOURCES
+5 vdc
+1.2 vdc
+2.5 vdc
+1.8 vdc
+3.3 vdc
+5 VDC
VSTBY_+5 VDC
SP-1
DRIVER INTERFACE
Signals
TxD RxD
RTS CTS CD
TxCLKO
TxCLKI
Protocols
ASYNC
SYNC
HDLC
SDLC
SP-2
DRIVER INTERFACE
SP-3
DRIVER INTERFACE
SP-5
DRIVER INTERFACE
Signals
TxD
RxD
TxCLKO
RxCLKI
Protocols
ASYNC
SYNC
HDLC
SDLC
SP-8
DRIVER INTERFACE
RxCLKI
BDM Bus
SP-1 Bus
SP-2 Bus
SP-3 Bus
SP-5 Bus
SP-8 Bus
P1 and P2 connectors
All signal are 5 VDC Level
SPI Bus
Power Fail Bus
USB Driver Bus
SP-4 Bus
SP-6 Bus
ENET 1 port 0 Bus
ENET 2 port 0 Bus
SPI
DRIVER INTERFACE
Signals
SPIMOSI SPIMISO SPICLK
SPICS1 SPICS2 SPICS3 SPICS4
DKEYPRESENT
POWER FAIL
DRIVER INTERFACE
+5 VDC
POWERUP
POWERDOWN
LINESYNC
CPURESET
CPUACTIVE
ENGINEPRESENT
USB V1.1
DRIVER INTERFACE
Signals
+USBD
-USBD
USB_PWR
USB_OVR
Option No. 8 or No. 9
SP-4
DRIVER INTERFACE
Signals
TxD
RxD
Protocols
ASYNC
SP-6
DRIVER INTERFACE
Signals
TxD
RxD
Protocols
ASYNC
Indicator LEDs
Populate only on Engine Board
ETHERNET No. 1
DRIVER INTERFACE
10/100 Mbits/S
Indicator LEDs
Populate only on Engine Board
ETHERNET No. 2
DRIVER INTERFACE
10/100 Mbits/S

This page was intentionally left blank

2.6 CONNECTORS' PIN OUT

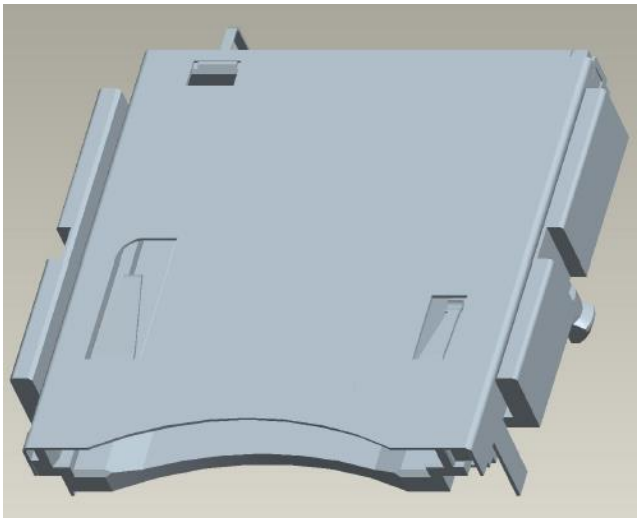
C13S Connector (DB25 Female):

Pin	Function
1	SP8_TxD+
2	SP8_RxD+
3	SP8_TxCLK+
4	SP8_RxCLK+
5	SP8_RTS+
6	SP8_CTS+
7	SP8_DCD+
8	N/A
9	LINESYNC+
10	NRESET+
11	POWERDN+
12	ISO+5VDC
13	ISOGND
14	SP8_TxD-
15	SP8_RxD-
16	SP8_TxCLK-
17	SP8_RxCLK-
18	SP8_RTS-
19	SP8_CTS-
20	SP8_DCD-
21	N/A
22	LINESYNC-
23	NRESET-
24	POWERDN-
25	FGND



SD Card Receptacle:

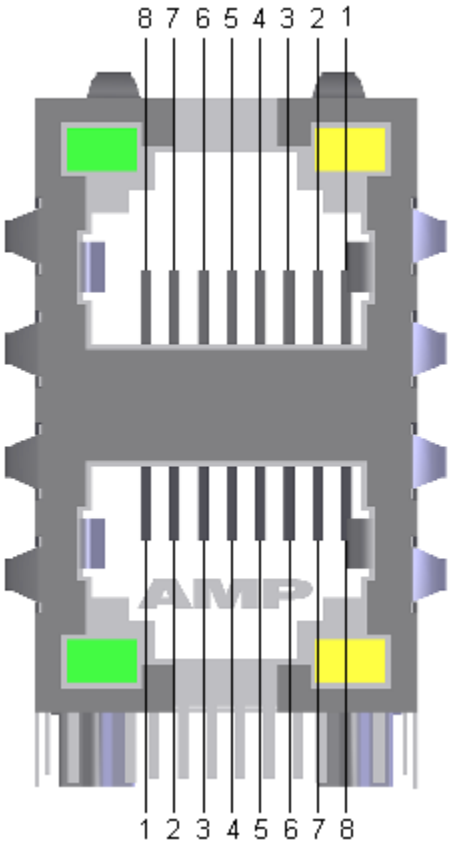
Pin	Function
1	CS/ DAT3
2	CMD/ MOSI
3	VSS
4	VDD
5	SD_CLK
6	VSS
7	DAT0/ MISO
8	DAT1
9	DAT2
10	CD_SW
11	CD_WP_COMMON
12	CD_WP
13	FGND
14	FGND
15	NC
16	NC



Ethernet Connector, ETH 1/1 (RJ45):

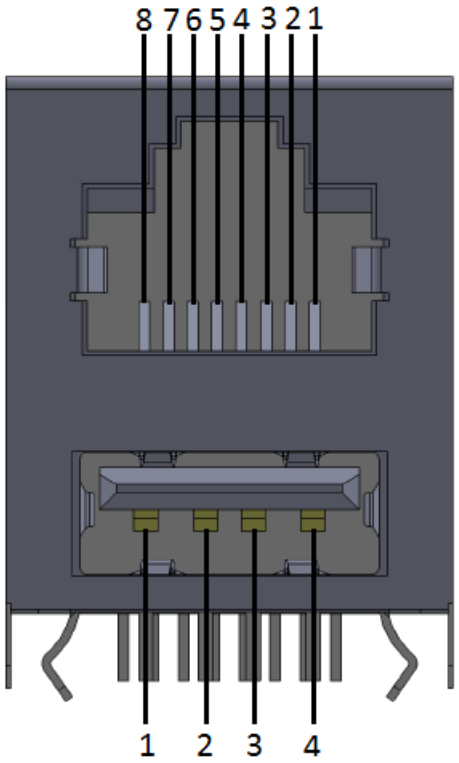
ENET 1 Port 1 (Up)	
Pin	Function
1	Tx+
2	Tx-
3	Rx+
4	Unused
5	Unused
6	Rx-
7	Unused
8	Unused

ENET 1 Port 2 (Down)	
Pin	Function
1	Tx+
2	Tx-
3	Rx+
4	Unused
5	Unused
6	Rx-
7	Unused
8	Unused



Ethernet Connector ETH 2 (RJ45):

ENET 2 Port 1 (Up)	
Pin	Function
1	Tx+
2	Tx-
3	Rx+
4	Unused
5	Unused
6	Rx-
7	Unused
8	Unused

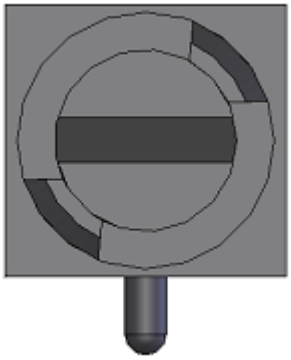


USB Connector:

Down	
Pin	Function
1	VCC
2	Data -
3	Data +
4	GND

Datakey receptacle connector:

Pin	Function
1	NC
2	Ground
3	VCC
4	NC
5	Data out
6	Chip select
7	Serial clock
8	Data in
9	Data in
10	Serial clock
11	Chip select
12	Data out
13	NC
14	VCC
15	Ground
16	NC
17	LOFO
18	LOFO



2.7 2070-1C MODULE DIMENSIONS

The 2070-1C CPU Module has the following dimensions:

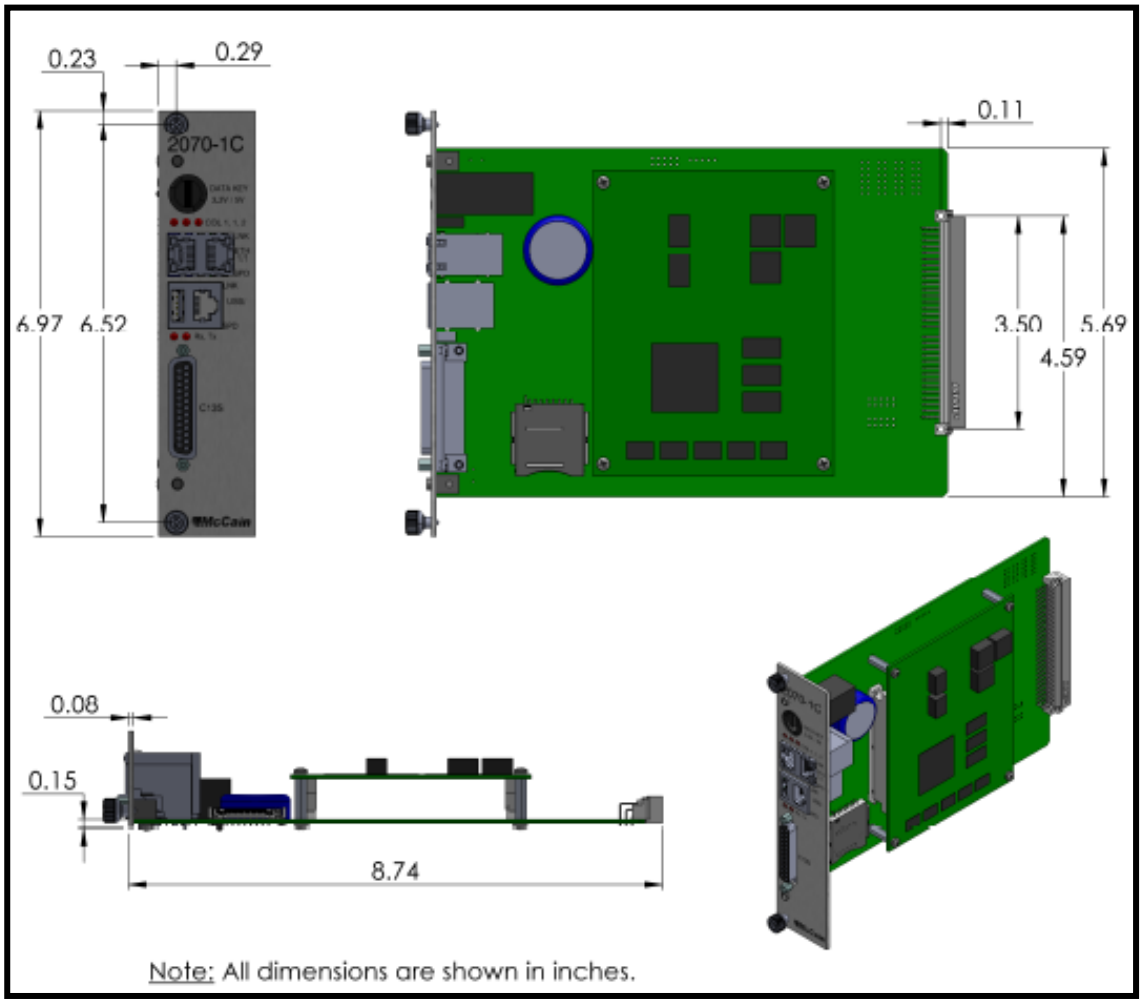


Figure 4: 2070-1C CPU dimensions.

2.8 ADJUSTMENT

The 2070-1C Module has no adjustments to be applied.

2.9 INSTALLING THE 2070-1C CPU MODULE

Follow these steps to complete the 2070-1C Module installation into the Controller.

Turn off the controller using the power switch located in the front plate of 2070-4A Module.

Slide the 2070-1C CPU into slot A5 thru the card guides. Press the module into the backplane and tighten the thumbscrews until the CPU module is secure.

3 2070-2E+ FIELD I/O MODULE

3.1 GENERAL DESCRIPTION

The 2070-2E+ Field I/O Module fully meets with the TEES 2009 and Errata 2 from December 5th 2014; it serves as an interface between the controller and the external world through its parallel I/O interface and two serial ports present at the front connectors.

The Field I/O module provides a parallel interface with 64 inputs/outputs present at C1S and C11S; also, a serial interface is provided through the SP-3 and SP-5 serial ports present at C12S connector, transmission and reception status indicators for both ports and a “SP-3 ACTIVE” port indicator are located at the front plate.

The Field I/O module is optically isolated from the rest of the 2070LX Controller.

The 2070-2E+ Field I/O Module consists of:

- C1S and C11S Connectors: Provides 64 inputs and 64 outputs for control of equipment.
- C12S Connector: Provides the SP-3 and SP-5 serial ports, the control signals LINESYNC, NRESET and POWERDOWN, and +5VDC ISO.
- A 2070 Type main board: Contains all necessary circuitry for implementing the 2070-2E+ functions.
- A 4X face plate: Provides mechanical support and identification in the Controller.

Figure 5: 2070-2E+ Module

3.2 THEORY OF OPERATION

The Field I/O module provides the interface between the controller and the external world, so that it contains all hardware and software needed for performing its functions as established into the TEES 2009 and Errata 2 from December 5th 2014.

The module contains a processor, SRAM, FLASH, parallel input/output ports, muzzle jumper, serial communication circuitry, C1S, C11S and C12S connectors installed on the front panel plate; serial communication circuitry, power Supply (+12VDC and +5VDC); and required software.

Processor

It is a Freescale MC68LC302 Integrated Multiprotocol Processor; it has a static 68008 core and a flexible communications architecture. The processor is running at 20MHz generated by an external oscillator.

Memory

SRAM

The 4Mbit Static RAM is used to execute code, store and retrieve all variable and temporary data.

It uses an 18-bit address bus (A0 to A17) and a 16-bit data bus (I/O 0 to I/O 15).

There is a glue logic stage to decode the signals from the control bus and handle the SRAM; this stage receives the signals and generates the proper signals for enabling the SRAM, for selecting the read/write operations and for selecting the low byte or upper byte.

FLASH

A 4Mbit FLASH memory is used in order to store the firmware. It is a non-volatile memory and serves as a media for storing program code and nonvolatile data so that if power is removed the stored data is not lost.

It uses an 18-bit address bus (A0 to A17) and a 16-bit data bus (I/O 0 to I/O 15).

Control signals

The control signals POWERUP, POWERDOWN and LINESYNC are signals coming from the Power Supply and are generated according to the conditions of the AC input power; CPURESET is a signal coming from the CPU and it is a software reset. They are received through the A3 slot; all are inverted and isolated before using them as follow:

POWERUP and CPURESET:

- These signals are OR'ed at the isolation stage, resulting into the NRESET signal.
- It enables a buffer gate to generate a reset signal that goes to the microprocessor and FLASH memory.
- It is converted to EIA-485 differential signals and routed to the C12S connector.

LINESYNC:

- Once the LINESYNC is isolated it is inverted again, then the inverted and not-inverted signals go to the processor.
- It is converted to EIA-485 differential signals and routed to the C12S connector.

POWERDOWN:

- It is converted to EIA-485 differential signals and routed to the C12S connector.

SP-3 and SP-5 Serial ports

SP-5

The module receives the SP-5 transmission signals (TxD and TxC) through the A3 connector; they are converted from EIA-485 signals to single ended signal, inverted and converted to multidrop isolated ports, then one is routed to the processor and the other one is converted to EIA-485 signals again then routed to the C12S connector mounted on the front plate.

The SP-5 reception signals (RxD and RxC) come from the C12S connector; they are converted from EIA-485 signals to single ended signal, opto-isolated, converted to differential signals and then routed to the A3 connector.

Field SP-5 enable signal (FSP5_EN): This signal disables the EIA485 line driver for the SP-5 reception signals (RxD and RxC) that come from the C12S connector and at the same time it enables the SP-5 reception signals (RxD and RxC) from the processor's communication port in order to send them to the A3 connector.

SP-3

The module receives the SP-3 transmission signals (TxD and TxC) through the A3 connector; they are converted from EIA-485 signals to single ended signal, inverted, isolated, converted to EIA-485 signals again then routed to the C12S front connector.

The SP-3 reception signals (RxD and RxC) come from the C12S connector; they are converted from EIA-485 signals to single ended signal, opto-isolated, converted to differential signals and then routed to the A3 connector.

- SP-3 enable switch (S1):

  The "S1" toggle switch located on the main board connect/disconnect the transmission and reception of the SP-3 serial port in the Field I/O module in order to prevent a multiple use.

  The switch enables/disables the EIA-485 line driver and receiver that handle this serial port by forcing the enable input to ground.

  Switch at "ON" position, SP-3 is available at C12S connector, "SP3 ACTIVE" LED is turned on.

  Switch at "OFF" position, SP-3 is NOT available at C12S connector, "SP-3 ACTIVE" LED is turned off.

LED’s status indicators

The status indicator circuits for transmission and reception consist of an inverter gate, an LED and a current limiting resistor in series.

- The “SP3 Tx” and “SP5 Tx” LED status indicator circuits are driven by the corresponding single ended transmission signal already isolated.
- The “SP3 Rx” and “SP5 Rx” LED status indicator circuit are driven by the corresponding single ended reception signal coming from the EIA-485 receiver at the isolated side.
- The “SP3 ACTIVE” status indicator circuit consists in a current limiting resistor and an LED; it is driven by the “S1” toggle switch. Indicator is turned on when switch is at “ON” position and turned off when the switch is at the “OFF” position.
- The “ACTIVE” LED status indicator circuit for the SP-5 consists of an LED and current limiting resistor in series; this circuit is driven directly by the microcontroller.
    - The Fast Flash (10Hz) condition means that the SP-5 communication is present.
    - The Slow Flash (1Hz) condition means that the SP-5 communication is not present.
    - If there is a steady condition either “ON” or “OFF” then there is a fault condition.

RESET

Processor has two input pins called /HALT and /RESET which are tied handled by the line /RESETH, when this line is in LOW state then processor is said to be RESET. There are four sources for generating the /RESETH line, the watchdog circuit, the supervisory circuit, the NRESET circuit and the BDM circuit.

Watchdog

A watchdog circuit is used to force a system reset and protect against system failures when the program is not executed as expected. This circuit provides a means to escape from unexpected input conditions, external events, or programming errors. The watchdog counter is cleared by the program periodically so that it never reaches its timeout value, otherwise a system failure occurred and then a system reset is applied to force the system back to a known starting point.

The circuit is implemented by using a D-Type flip—flop that receives two inputs from the processor (watchdog control and the watchdog reset lines), its output (watchdog flag) goes to the watchdog input at processor.

The watchdog control input presets the output to LOW state; watchdog reset serves as a clock input transferring the input to the output, forcing the output to HIGH state because the input is tied to ground. Watchdog flag keeps the watchdog status and it is monitored by the processor after the reset condition in order to know if it was because a watchdog “no service” condition as a result of a program malfunction.

WDT enable shunt:
A watchdog timer enable shunt is provided on the module. It consists of a 3-positions header (JP1) and a jumper to be placed at either ON or OFF position.

- Jumper at ON position (pin-1 to pin-2): The processor outputs a state change on OUTPUT 39 (Monitor Watchdog Timer Input) every 100ms for 10 seconds or due to Set Output Command. The watchdog output is sent to the output port #5 bit 8 and located at C1S connector pin-103.

- Jumper at OFF position (pin-2 to pin-3): Causes no watchdog output. This feature is required to operate with the Model 210 Monitor Unit.

Supervisory circuit

The supervisory circuit monitors the power supply of the processor and it asserts a reset if the power supply drops below the threshold level of 4.63 VDC. The reset is an active low output that remains low by 140ms once power supply reaches the threshold level.

NRESET

This signal is the result of OR'ing the POWERUP and CPURESET signals at the isolation stage.

POWERUP is a signal from the Power Supply and is generated according to the conditions of the AC input power; it is asserted if a power failure lasts more that 525ms ±25ms.

CPURESET is a signal coming from the CPU and it is a software reset.

They are received through the A3 slot, inverted, OR'ed and isolated. The NRESET signal enables a buffer gate to generate the /RESETH signal that asserts the reset pin at processor.

BDM port

There is a 10-positions connector header (BDM) on the main board and it is used as a manufacturer-specific BDM interface port for in-circuit programming and test on-board devices.

Parallel I/O ports

The parallel I/O ports consist of 64 input and 64 outputs that are present at the front connectors C1S and C11S, see CONNECTOR's PIN OUT section to see physical correspondence.

The front connectors are located on the connector board which is plugged to the main board through a 150-positions receptacle connector, so that the 64 inputs and 64 outputs reach the main board and are routed to their corresponding circuits.

Parallel inputs ports

64 inputs using ground-true logic are provided; each input has an internal 10KOhm pull-up resistor to the ISO +12VDC and a resistive network in order to adequate the signal so that the input is a logic "1" when the input voltage at its field connector input is less than 3.5VDC, and is logic "0" when the input voltage exceeds 8.5VDC.

The 64 inputs are distributed on eight octal buffers / line drivers; in order to send these inputs to the processor they are arranged into four 16-bit groups called input banks.

Each input bank is formed of two octal buffers, receives 16 inputs from the resistive network and sends the corresponding 16-bits of information to the CPU through the data bus when its corresponding enable input is asserted.

Bank 1 (formed by port 1 and port 2) handle the inputs 1 to 16.

Bank 2 (formed by port 3 and port 4) handle the inputs 17 to 32.

Bank 3 (formed by port 5 and port 6) handle the inputs 33 to 48.

Bank 4 (formed by port 7 and port 8) handle the inputs 49 to 64.

This lines for enabling and disabling the four input banks come from a 3-line to 8-line decoder. The decoder accepts the lines A1, A2 and A3 from the address bus to select a bank, two active-low enable inputs for the chip select and output enable and one active-high enable input for the line that clear the output banks.

The parallel input ports' stage is powered with ISO +5VDC.

Parallel outputs ports

64 outputs using ground-true logic are provided; outputs written as a logic "1" have sink-current capability and outputs written as a logic "0" provide an open circuit. Each output is capable of driving 50 VDC and sinking 150mA.

The 64 outputs are distributed on eight octal D-Type latches; in order to send these outputs to the field connectors they are arranged into four 16-bit groups called output banks.

Each output bank is formed of two octal D-Type latches, receives 16-bits of information from the CPU through the data bus and sends the corresponding 16 outputs to the field connectors at the positive edge of the clock input.

Bank 1 (formed by port 1 and port 2) handle the outputs 1 to 16.

Bank 2 (formed by port 3 and port 4) handle the outputs 17 to 32.

Bank 3 (formed by port 5 and port 6) handle the outputs 33 to 48.

Bank 4 (formed by port 7 and port 8) handle the outputs 49 to 64.

This lines for enabling and disabling the four output banks come from a 3-line to 8-line decoder. The decoder accepts the lines A1, A2 and A3 from the address bus to select a bank, two active-low enable inputs for the chip select and output enable and one active-high enable input for the line that clear the output banks.

The line for enabling/disabling the output banks is connected to the clock input pin of the corresponding octal D-Type latch, when this input goes to high, information at the inputs are transferred to the outputs on the positive going edge of the clock pulse. When the clock input is at either the high or low level, the input signals have no effect at the outputs.

The parallel output ports' stage is powered with ISO +5VDC.

Connectors

150-Positions header
This is a 150-pins high density 2mm male header connector used to interconnect the main board (which support all of the input/output, power, isolation and control circuitry) and the connector board (which support all of the necessary connectors for the field interface) that has the mating female receptacle.

A3 Connector
It is a 96-pin right angle DIN connector used to interface the Field I/O module to the serial mother board.

It carries the signals and power lines for:

- The serial ports SP-3 and SP-5.
- The control signals: LINESYNC, POWERUP, POWERDOWN and CPURESET.
- The +5VDC voltage that is used to feed the circuitry at the non-isolated side, the line driver and line receiver, the inverter gates, the opto-isolators and the toggle switch.
- The +12VDC ISO voltage that is then converted to +5VDC ISO in order to feed all Control and I/O circuitry.

Isolation Stage

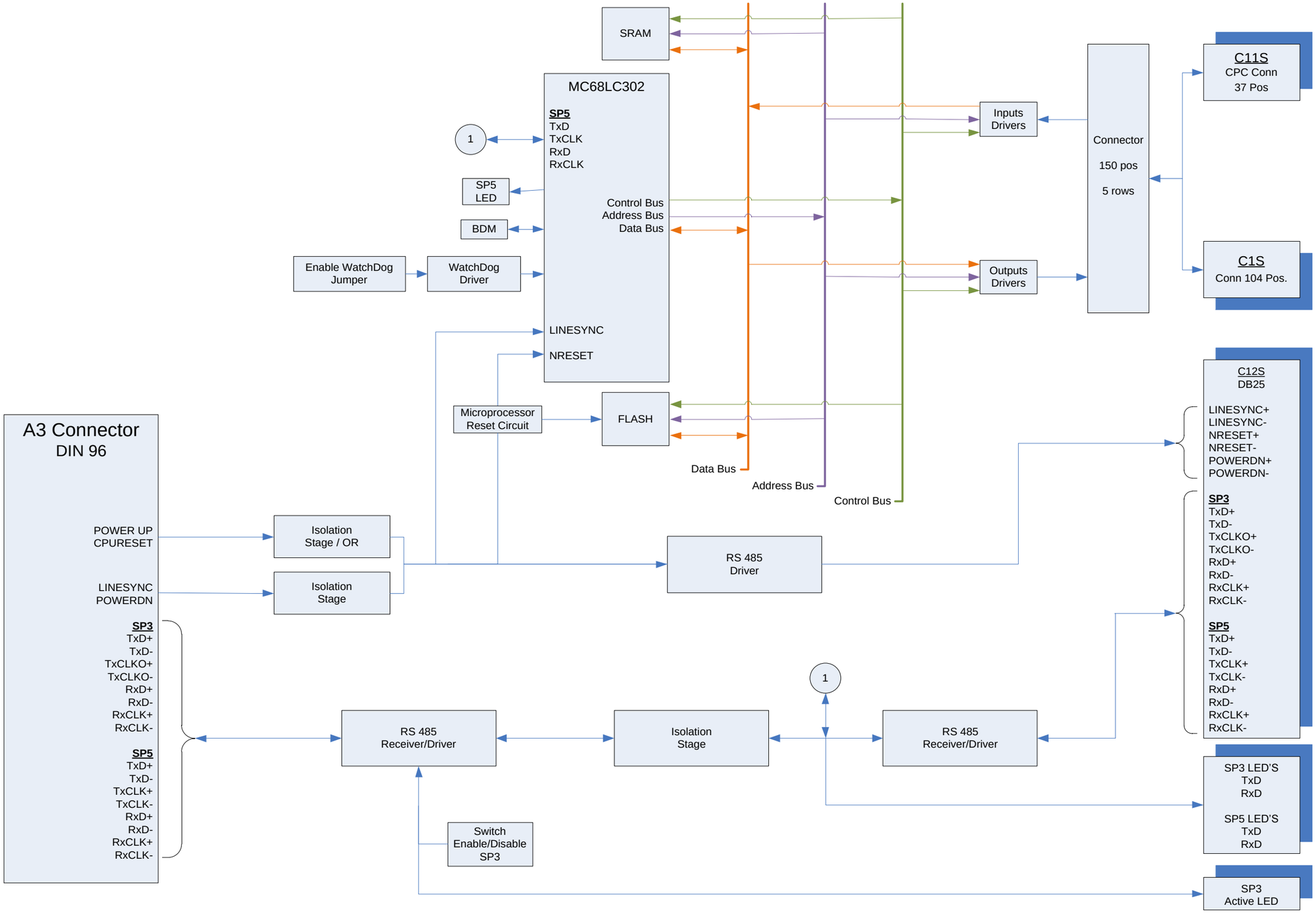
The Field I/O module is the module for interfacing the Controller with the real world so that it is isolated from the system in order to avoid all kind of problems related to the field such as ground loops, induced noise, etc.

The module optically isolates the transmission and reception lines of serial ports SP-3 and SP-5; therefore, all communication lines between the CPU and Field I/O module are isolated.

The serial ports come from the CPU through the Serial Motherboard and are present at A3 connector; the RS485 communication signals entering to the Field I/O module are converted to single ended lines and are then isolated; also, the communication lines going to the CPU are isolated and then converted to RS485 signals. The isolation is achieved by using optically coupled logic gates that combine a light emitting diode and a photo detector. The detector's output is an open collector transistor. This stage provides circuit isolation and high speed logic interfacing at induced noise environments.

The Control and I/O circuitry is fed with +5VDC ISO, that is obtained from the ISO +12VDC coming from the 2070-4A Power Supply and present at A3 connector.

3.3 2070-2E+ BLOCK DIAGRAM

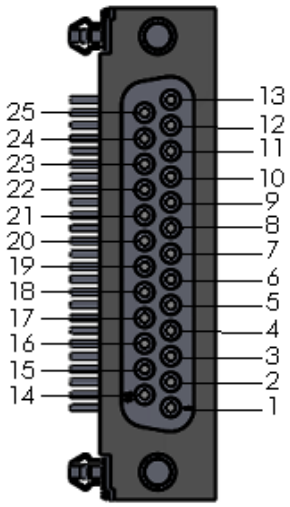


This page was intentionally left blank

3.4 CONNECTORS' PIN OUT

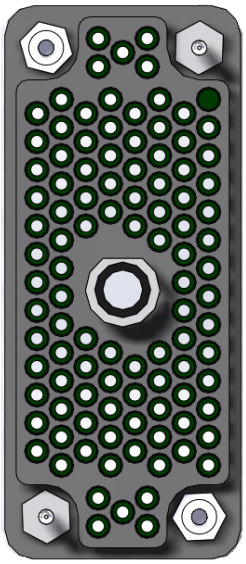
Connector C12S (DB25 Female):

Pin	Function	Pin	Function	Pin	Function
1	SP5 TxD+	11	POWERDN+	21	SP3 RxCLK-
2	SP5 RxD+	12	ISO VCC	22	LINESYNC-
3	SP5 TxCLK+	13	ISO GND	23	NRESET-
4	SP5 RxCLK+	14	SP5 TxD-	24	POWERDW-
5	SP3 TxD+	15	SP5 RxD-	25	FGND
6	SP3 RxD+	16	SP5 TxCLK-		
7	SP3 TxCLKO+	17	SP5 RxCLK-		
8	SP3 RxCLK+	18	SP3 TxD-		
9	LINESYNC+	19	SP3 RxD-		
10	NRESET+	20	SP3 TxCLKO-		



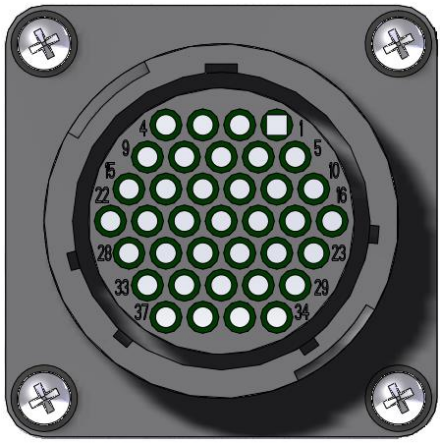
Connector C1S:

Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	DCG #2	27	O24	53	I14	79	I44
2	O0	28	O25	54	I15	80	I45
3	O1	29	O26	55	I16	81	I46
4	O2	30	O27	56	I17	82	I47
5	O3	31	O28	57	I18	83	O40
6	O4	32	O29	58	I19	84	O41
7	O5	33	O30	59	I20	85	O42
8	O6	34	O31	60	I21	86	O43
9	O7	35	O32	61	I22	87	O44
10	O8	36	O33	62	I23	88	O45
11	O9	37	O34	63	I28	89	O46
12	O10	38	O35	64	I29	90	O47
13	O11	39	I0	65	I30	91	O48
14	DCG #2	40	I1	66	I31	92	DCG #2
15	O12	41	I2	67	I32	93	O49
16	O13	42	I3	68	I33	94	O50
17	O14	43	I4	69	I34	95	O51
18	O15	44	I5	70	I35	96	O52
19	O16	45	I6	71	I36	97	O53
20	O17	46	I7	72	I37	98	O54
21	O18	47	I8	73	I38	99	O55
22	O19	48	I9	74	I39	100	O36
23	O20	49	I10	75	I40	101	O37
24	O21	50	I11	76	I41	102	O38 DET RES
25	O22	51	I12	77	I42	103	O39 WDT
26	O23	52	I13	78	I43	104	DCG #2



Connector C11S:

Pin	Function	Pin	Function
1	O56	20	I53
2	O57	21	I54
3	O58	22	I55
4	O59	23	I56
5	O60	24	I57
6	O61	25	I58
7	O62	26	I59
8	O63	27	I60
9	DCG #2	28	I61
10	I24	29	I62
11	I25	30	I63
12	I26	31	DCG #2
13	I27	32	NA
14	DCG #2	33	NA
15	I48	34	NA
16	I49	35	NA
17	I50	36	NA
18	I51	37	DCG #2
19	I52		



3.5 2070-2E+ MODULE DIMENSIONS

The 2070-2E+ Field I/O has the following dimensions

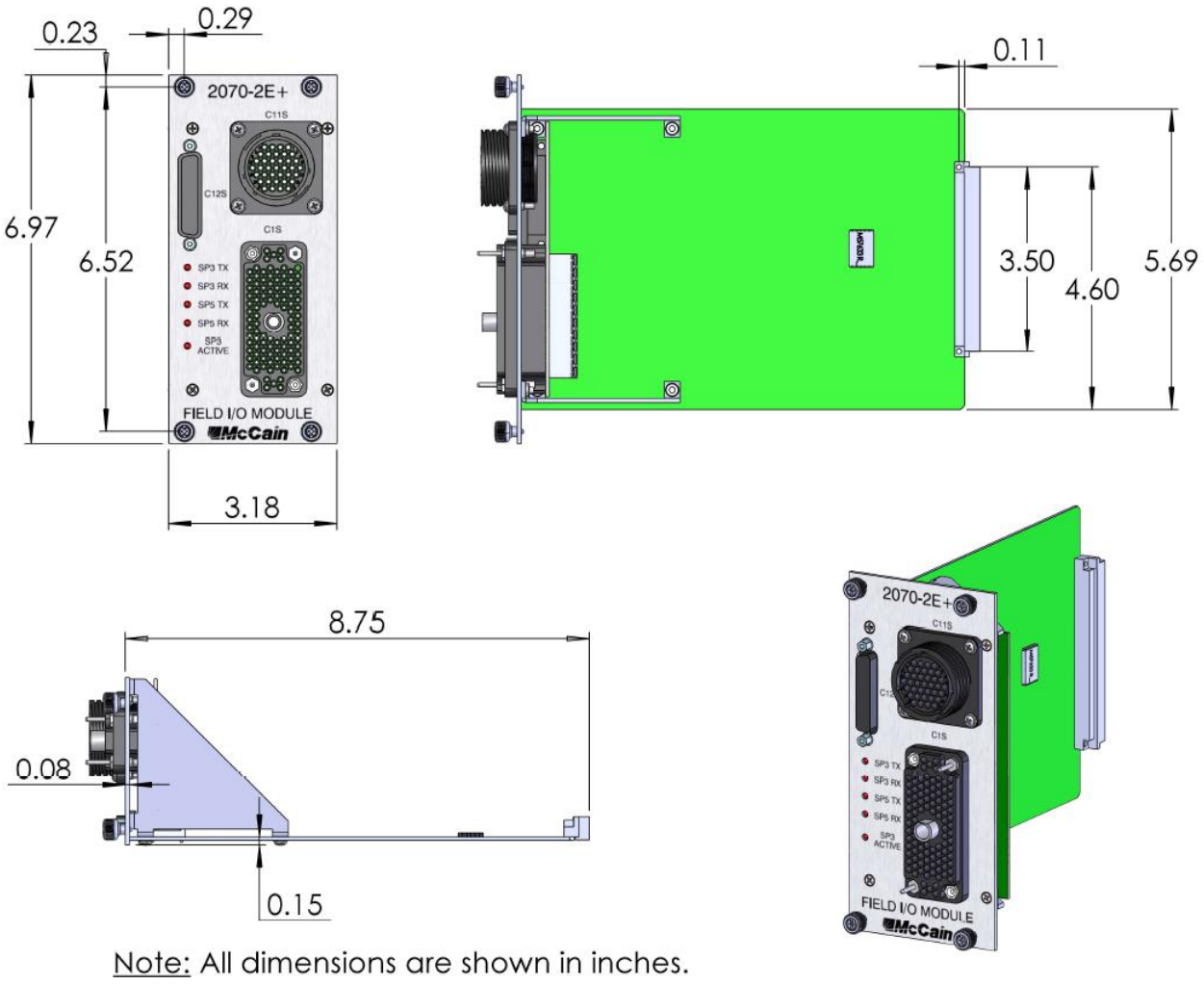


Figure 6: 2070-2E+ Dimensions

3.6 INSTALLING THE 2070-2E+ MODULE

Normally the module is attached to the controller, but this section contains information of installation of the 2070-2E+ in case it is not.

1. Turning off the controller using the power switch located in the front plate of 2070-4A Module.
2. Slide the 2070-2E+ into slot A3 thru the car guides. Press the module into the backplane; tighten the thumbscrews until the module is secure.

These steps complete the 2070-2E+ installation into the 2070LX Controller.

4 2070LX MODULE, FRONT PANEL ASSEMBLY

4.1 GENERAL DESCRIPTION

The Front Panel Assembly (FPA) provides a user interface via keypads and the LCD display, also the module has the serial port SP-4 available through the C50S and C50J connectors for a terminal's connection. Also an ACTIVE LED to show the application's status, an AUX switch and a LCD's contrast knob are available. The Front Panel assembly also serves as a swinging door to cover the back of the Chassis and the Serial motherboard when closed.

The assembly consists of:

- An 8 line by 40 character display and a LCD's contrast knob.
- Keyboard interfaces: a 4x4 alphanumeric keyboard and a 3x4 cursor and symbol keyboard.
- C50S and C50J connectors: Provides a connection to the SP-4.
- An AUX switch.
- An ACTIVE LED.
- A P2 connector: for interfacing the PCB assembly to the LCD display.
- A P3 connector: for interfacing the module to the CPU through the Serial motherboard.
- A RESET switch: for a manual reset of the Front panel assembly.
- A sliding latch and latch guide.
- Two thumbscrews for a mechanical attachment to the Chassis unit.
- A sub-assembly board: contains all necessary circuitry for implementing the FPA functions.
- A metal panel: provides mechanical support, necessary cutouts and identification.

The Figure 7 shows the 2070LX module.

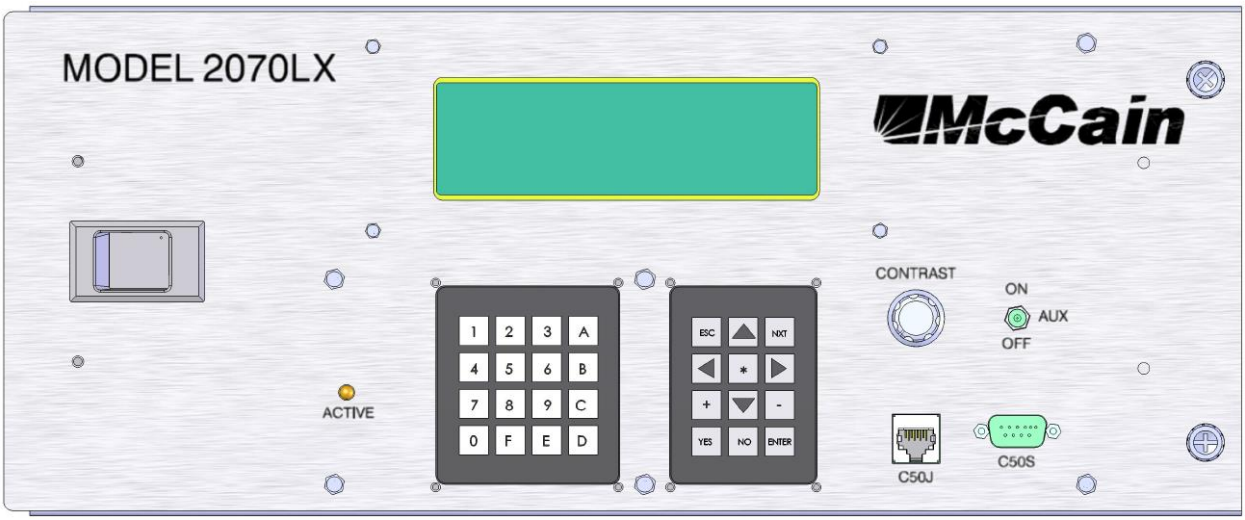


Figure 7: 2070LX Module

4.2 THEORY OF OPERATION

Microcontroller

The FREESCALE M9S12E64 runs at 24.576MHZ and performs all necessary functions of the Front Panel assembly: communicates to the CPU via the serial asynchronous port SP-6, scans the keypads and displays messages on the LCD display, controls the LCD backlight, generates the BELL signal, monitors the AUX switch and the manual RESET switch.

Keyboards

The keyboard interface is comprised of a 4x4 keyboard (sixteen keys for hexadecimal alphanumeric entry) and a 3x4 keyboard (twelve keys for cursor control and symbol entry).
All of the lines connected to these two keyboards go directly to the M9S12E64 microcontroller.

P2 and P3 connectors

P2: This 16-positions connector is the interface from the FPA's PCB assembly to the LCD display. It carries the data and command lines from microcontroller to the LCD unit, the intensity control from the contrast knob and the backlighting control.

P3: This 40-positions connector is the interface to the Serial motherboard in order to connect the communications lines for the SP-6 port and SP-4 port and the control lines ACTIVE LED and RESET coming from the CPU.

C50S/ C50J Connectors

The C50S is a 9-positions D-sub female connector and the C50J is a RJ-45 Ethernet jack connector. Both of this connectors provide the asynchronous serial port SP-4 from the CPU to be used as a terminal's connection and the C50 enable line that serves to sense if the C50S/C50J connectors are being used or not, this prevents the SP-4 port be used at the same time on the front connector and at A1 connector on Serial motherboard.

SP-4 circuitry

The related circuitry consists of one RS-232 transceiver and two RS-485 transceivers that implement the interface for transmitting and receiving data to and from the SP-4 coming from the CPU.

The RS-485 transceiver receives the SP-4 transmission differential signals coming from the P3 connector and converts them to a single end signal; this signal enters to the RS-232 transceiver whose output is connected to the Tx pin at the C50S/C50J connectors.

The Rx pin at C50S/C50J connectors receives the SP-4 reception signal and route it to the RS-232 transceiver whose output is connected to the RS-485 transceiver, then the differential signals are then routed to the P3 connector.

The C50 enable circuit

This line is normally forced to High state through a 10K pull-up resistor to Vcc; it is connected to the driver's input of a RS-485 transceiver whose differential outputs are connected to the enable pins of the RS-485 transceiver that handle the SP-4 communication; while the driver's input is high, the enable inputs disable the SP-4 communications and the C50 enable signal goes to high, this signal is one of the differential outputs and it is routed to P3 connector.

Bell

It is an electronic bell controlled by the microcontroller used to signal receipt of ^G (hex 07) and RESET condition. It is performed by a buzzer which is managed by the microcontroller applying a 2 KHz square signal for a period of 350mS.

AUX Switch

This is a toggle switch that forces the status of the STOPTIME line from microcontroller to Low by connecting a pull-up to logic ground. The microcontroller receives the status of this line and sends a code to the CPU through the P3 connector; this information is used according to the application running in CPU.

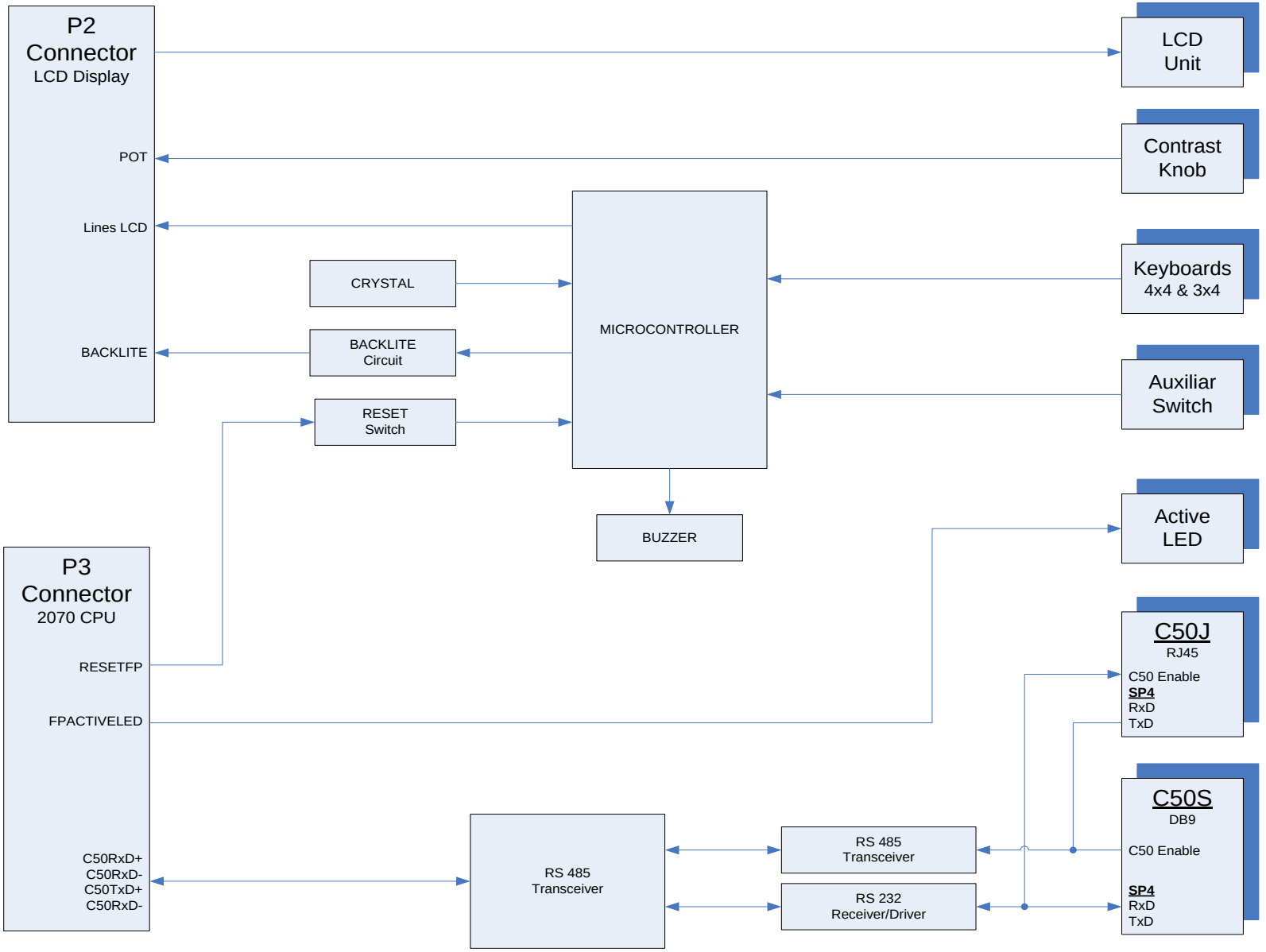
RESET Switch

It is a push-button switch located on the back of the FPA on the PCB sub-assembly. It serves as switch that once touched it momentary pulls down a line monitored by the microcontroller which then reset the operation and also sends a reset the LCD through the P2 connector.

ACTIVE LED

An LED with a series resistor connected to Vcc is activated by the CPU through the P3 connector. This LED is normally used to indicate the status of the application running in the CPU.

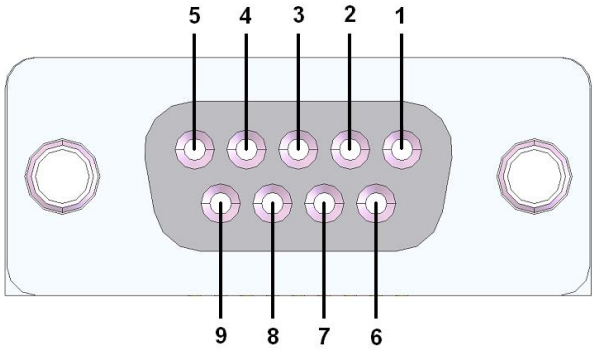
4.3 2070LX BLOCK DIAGRAM



4.4 CONNECTORS' PIN OUT

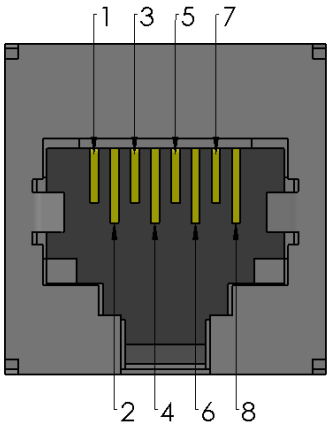
Connector C50S (DB9 Female):

Pin	Function
1	C50 Enable
2	SP4 RxD
3	SP4 TxD
4	nc
5	DCG #1
6	nc
7	nc
8	nc
9	nc

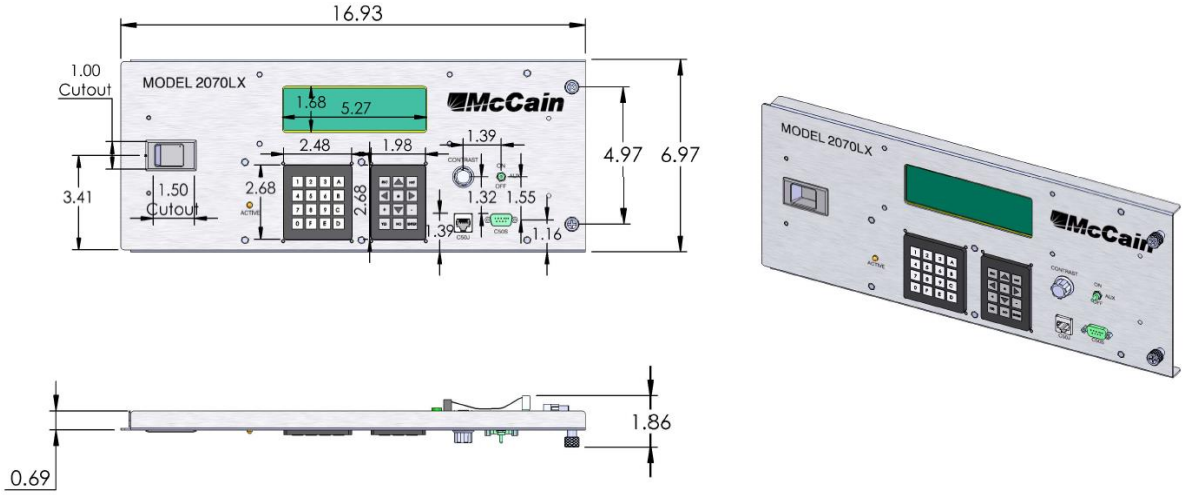


Connector C50J (RJ45):

Pin	Function
1	C50 Enable
2	SP4 RxD
3	SP4 TxD
4	Nc
5	DCG #1
6	Nc
7	Nc
8	Nc
9	Nc



4.5 2070LX MODULE DIMENSIONS



Note: All dimensions are shown in inches.

Figure 8: 2070LX Dimensions

4.6 ADJUSTMENT

The only adjustment available on the Front Panel Assembly is the LCD contrast that can be adjusted in accordance with user's needs through the contrast knob.

4.7 INSTALLING THE 2070LX

Normally the controller has the 2070LX assembly, but this section contains information of installation of the 2070LX in case it is not.

1. Turn off the controller using the power switch located in the front plate of 2070-4A Module.
2. Install on the front of the controller and attach to the chassis' hinge through the two thumbscrews on the right side and secure it through the latch slide on the left side.
3. Tighten the thumbscrews until the module is secure.
4. Insert the 40-position ribbon plug connector from the Serial motherboard into the P3 Connector.
5. Make sure the 2070LX is correctly opened, closed and secured.

These steps complete the 2070LX installation in the Controller.

5 2070-4A POWER SUPPLY MODULE

5.1 GENERAL DESCRIPTION

The model 2070-4A is the Power Supply module of the Controller. It receives the AC line through the AC cord and provides all necessary power outputs and signal outputs at PS1 and PS2 connectors.

The power lines are +5VDC @ 10A, +/-12VDC @ 0.5A, isolated +12VDC @ 1A and the +5VDC Standby power; and control signals are LINESYNC, ACFAIL/POWER DOWN and POWER UP/SYSTEM RESET.

The module is constructed in accordance to the TEES 2009. It is a self-contained, vented only by convection. The control board and small power supply modules are enclosed by two side plates and one rear plate forming a cage with the top and bottom not covered and used for ventilation purposes.

The Power supply module consists of:

- PS1 and PS2 connectors: Provides the interface for all power and signals needed by the controller.
- LED indicators: They are ON when voltage is within tolerance, otherwise they are OFF.
- ON/OFF Power switch: Provide for turning ON and OFF the module.
- Slow Blow fuse: Provided to protect the module in case of exceeding the current limit.
- 15 inches of AC Cord and cord wraps to stow the cord when not in use.
- A sub-assembly control board: contains all necessary circuitry for implementing the Power Supply module functions.
- Small power supply modules that provide all necessary power.
- Harnessing: for interconnecting the small power modules to the control board.
- Metal panels: provides mechanical support, necessary cutouts and identification.

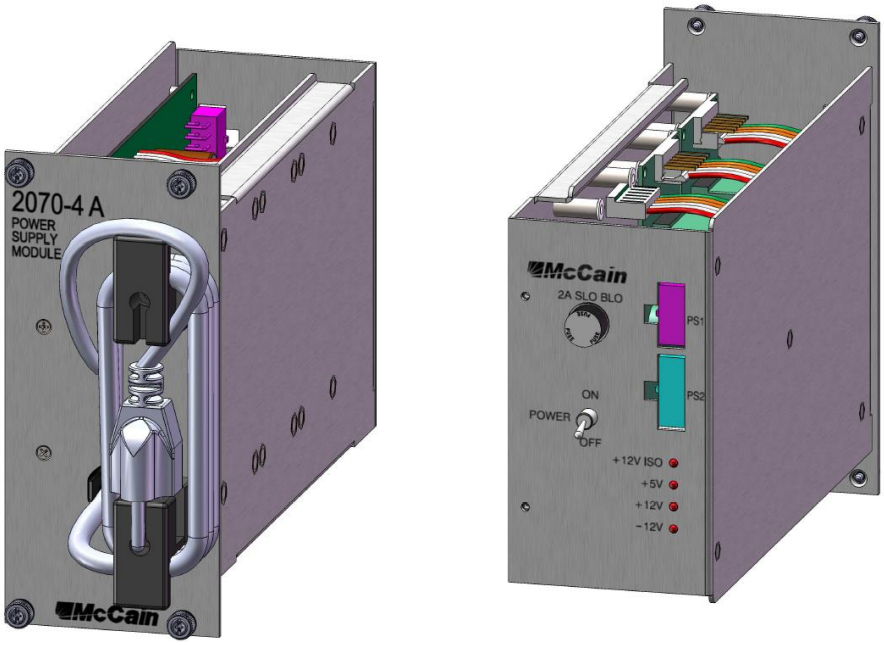


Figure 9: Power Supply 2070-4A

5.2 THEORY OF OPERATION

The 2070-4A Power Supply module consists of several sub-systems that perform different functions in order to meet the requirements listed on TEES 2009.

This section provides a little insight of the sub-systems' functionality.

AC Input, Fuse and Switch

The AC line is fed to the Power Supply from the AC cord to the AC INPUT header providing the Hot, Neutral and Earth lines to the input protection circuitry. The Hot line is routed from the AC INPUT header to the 2A fuse and then to the switch, the next stages are the input protection and the EMI filter.

Input protection

The input protection consists of the next:

- Two 1.5Ohms 15W resistors, one placed on the AC+ line and the other one on the AC- line.
- Three surge arrestors placed between AC+ and AC-, AC+ and EG, AC- and EG.
- One .68uF capacitor located between AC+ and AC-, between the resistors and surge arresters.

EMI Filter

The EMI filter is contained into a discrete device. It receives the AC input signal and delivers the power already filtered to the circuitry in the Power Supply module.

Power Supply Modules

The Power Supply filters the 120 VAC line and then feeds three power modules. These power modules generate the required voltage outputs:

- +5VDC module, is used for providing +5VDC.
- +12VDC module, is used for providing +12VDC and -12VDC (the -12VDC are obtained through a switching regulator on control board).
- +12VDCISO module, is used for providing +12VDCISO.

The Power Supply modules are connected to the Control board via a set of harnesses.

Zero-Crossing Detector circuit

This circuit is based on the MC33161P which is a universal voltage monitor with two comparator channels with hysteresis, a Mode Select Input, a pinned out 2.54V reference and two open collector outputs.

In order to preserve the isolation between the AC and DC signals, a transformer, a diode bridge and an electrolytic capacitor are used to generate 24VDC and feed the circuitry. Also, two opto-isolators MOC8102 are used to isolate the outputs from the AC side to the logic side.

The AC+ line is separated through two resistor networks in order to attenuate it and also to generate a difference on AC voltage levels, and then the AC signal is feed to the inputs of the voltage monitor device as follow:

- Input 1 the resistor network connected to this input is around 510KOhms and it is connected to a 6V zener diode.
- Input 2 the resistor network connected to this input is around 998KOhms and it is connected to a voltage divider in parallel to a 6V zener diode.

The voltage level at one zener feeds a voltage divider including a potentiometer; this voltage divider is very sensitive and sets the trigger level for the comparator at input 2. It is used for factory adjustment to start operation when the AC line reaches the recovery voltage level, for this model 85VAC.

The outputs of the M33161P (OUT1 and OUT2) are routed to two opto-isolators controlling them at the cathode side, so that they are activated according to the zero crossing points of each AC input network. These two isolated signals become the CLOCK and CLEAR signals for the D-Type Flip-Flop whose output is a pulse synchronized to the AC input line called AC monitor.

AC monitor

This signal is generated at the D-type flip-flop which is receiving the alternating signals coming from the opto-isolators at the CLOCK and CLEAR inputs, one input sets the output and the other input clears the output; the generated pulse is synchronized to the AC line because of the zero-crossing detection circuit.

The pulse is monitored by the microcontroller becoming into an interruption, based on the presence or absence of this interruption, the microcontroller generates the control signals LINESYNC, ACFAIL, ACFAIL/PWR DOWN and PWR UP/SYS RESET.

The zero-crossing circuit is adjusted via the potentiometer to obtain this signal while the AC line is above the 85VAC, if the AC line goes below 85VAC then any valid pulse is generated and it is interpreted by the microprocessor as a power failure.

Microcontroller

The Power Supply control is handled by an 8-bit high performance Freescale microcontroller MC9S08QG8 running at 15.36MHz.

The microcontroller has the next tasks:

- Monitors the AC monitor interruption.
- Generate the control signals: ACFAIL/POWERDOWN, POWERUP/SYSTEMRESET and LINESYNC.
- Monitors the voltage levels through three ADC; +5VDC, +12VDC and -12VDC.
- Activates the LED indicators for three voltages; +5VDC, +12VDC and -12VDC.

DC Regulator

A 3.3VDC linear regulator is used in order to feed the microcontroller, oscillator and LED indicators.

Control signals

Upon the arrival of the AC Monitor signal to the microprocessor, it is the firmware that defines if this signal meets the necessary requirements to generate and maintain the control signals ACFAIL/POWERDOWN, POWERUP/SYSTEMRESET and LINESYNC. All these lines are generated by the microprocessor and go to the control signals' output stage.

The ACFAIL/POWER DOWN output lines transition to High at Power Restoration; these lines go Low (ground true) immediately upon Power Failure. These lines are driven separately.

The SYSRESET/POWERUP output Lines go to High 225 ± 25ms after power restoration and the supply is fully recovered; these lines go Low 525 ± 25ms after ACFAIL goes Low.

Power up sequence

After detecting the presence of the AC signal the microcontroller set the ACFAIL/PWR DOWN line to high; if there is no power failure within a 225ms period then the PWR UP/SYS RESET line is set to high.

Power down sequence:

During a power failure, the ACFAIL/PWR DOWN signal is set to Low immediately, if the power failure lasts more than 525 ± 25ms then the PWR UP/SYS RESET line is set to Low.

The LINESYNC signal is a continuous square wave signal of +5VDC amplitude, 8.333 ms half-cycle pulse duration, and 50 ± 1 % duty cycle; it is synchronized to the 60Hz VAC incoming power line at 120 and 300 degree. The LINESYNC signal begins when SYSTEMRESET signal transitions to High; this signal continues until SYSRESET transitions to Low. The microprocessor compensates for missing pulses during normal operation.

Control signals output stage

It is used for supplying the appropriate drive sink capability to the control signals on the PS connectors. This stage consists of two FET's and three resistors for each control signal, it is arranged for giving an output of the same logic level as the input; this is, if the control signal coming from the microcontrollers is HIGH then the output of this stage is also HIGH.

The Linesync output has a drive sink capability of 16 mA. A 2K ohm pull-up resistor is connected between the output and +5 VDC.

Voltage monitors

In order to monitor the voltage levels for +5VDC, +12VDC and -12VDC voltage dividers are arranged and connected to the microcontroller's ADC's, if the monitored levels are within range the LED status indicators are activated.

Voltage status indicators

A LED status indicator for each power supply is provided to indicate if the voltage levels are within range or not; The LED status indicator is ON if the voltage supply is within range and OFF otherwise: the +5 VDC is within 5% and the 12 VDC is within 8% of their nominal levels.

The LED DC POWER Indicator indicates that the required DC Voltage meets the following conditions: For the +5VDC, +12VDC and -12VDC supplies, the circuit consists of an LED in series with a 220 Ohms resistor, connected to +3.3VDC and activated by the microcontroller.

For the +12VDCISO supply, a discrete voltage monitor device is used. It monitors and indicates if the level is within range. In this case there is an LED with a 2.2KOhms series resistor connected to +12VDCISO and activated by this device.

Standby Power

+ 5 VDC STANDBY POWER is provided to hold up system devices during power down period. It consists of the monitor circuitry; hold up capacitors, and charging circuitry. A charging circuit is provided that under normal operation fully charges and float the capacitors. The Hold Up power requirements are a minimum constant drain of 600uA at a range of +5 to +2 VDC for over 10 hours.

It is achieved through the high efficiency positive voltage regulator ICL7663 and two 47F hold up capacitors plus charging circuitry.

Holdup time

The Power Supply module is able to deliver at least 30W for 550ms after the ACFAIL line is set to Low. It is capable of holding the unit for two 500ms power failure periods occurring in a 1.5 seconds period.

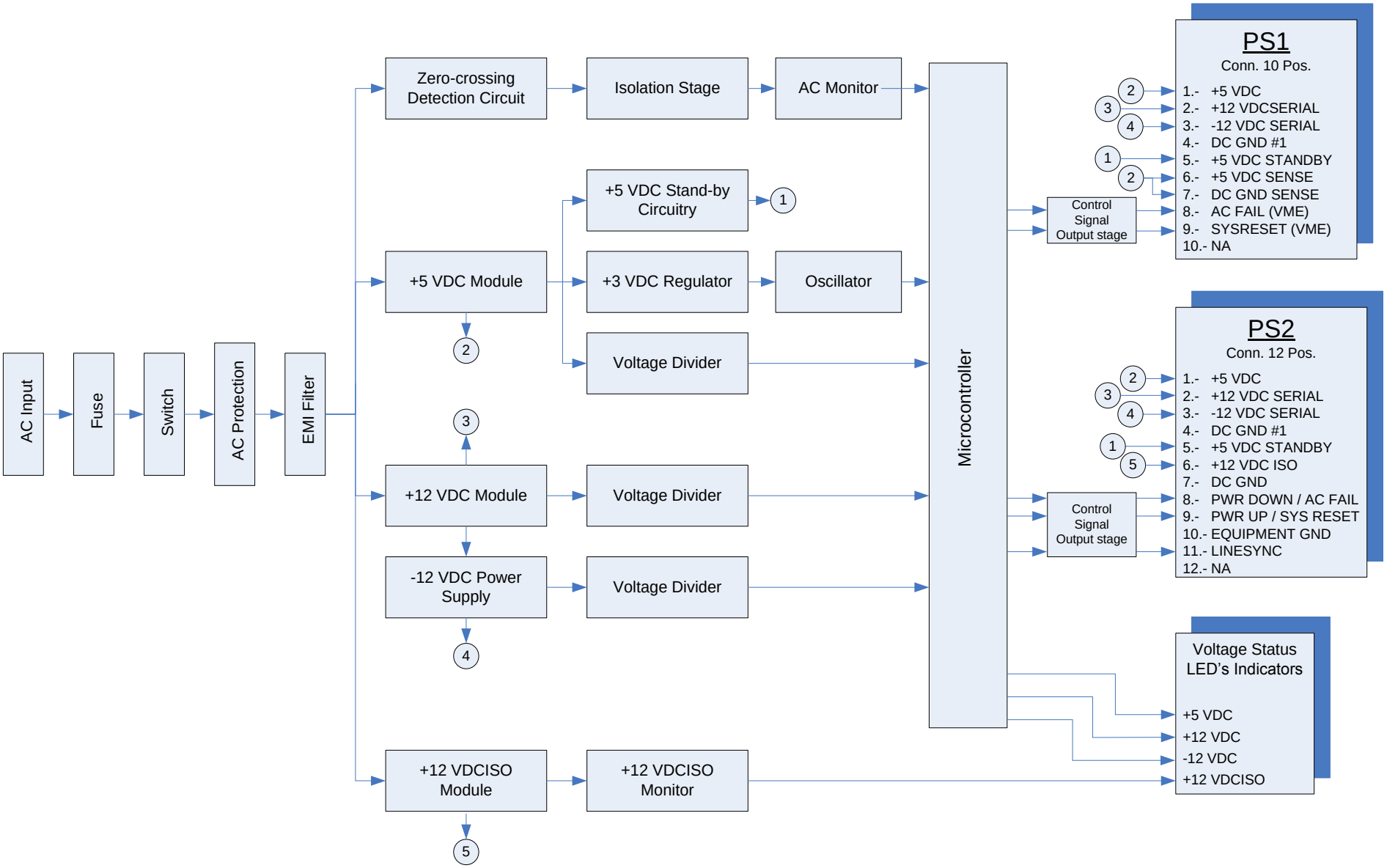
Power Supply requirements

These are the electrical specifications of Power Supply Module.

Voltage	Tolerances	I MIN	I MAX
+5 VDC	+4.875to +5.125 VDC	1.0 AMP	10.0 AMP
+12 VDC Serial	+11.4 to +12.6 VDC	0.1 AMP	0.5 AMP
-12 VDC Serial	-11.4 to –12.6 VDC	0.1 AMP	0.5 AMP
+12 VDC	+11.4 to +12.6 VDC	0.1 AMP	1 AMP

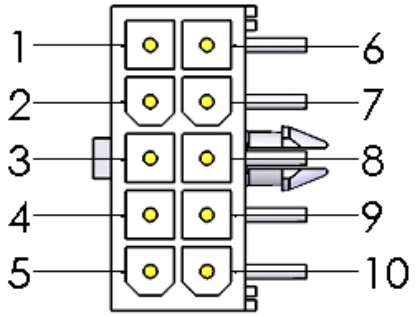
Line / Load Regulation	Meets the table tolerances values for voltage range of 95 to 135 VAC, minimum and maximum loads called out in the table and including ripple noise.
Efficiency	70 % minimum
Ripple & Noise	Less than 0.2 % rms, 1% peak to peak or 50 mV Whichever is greater
Voltage Overshoot	No greater than 5 %, all outputs
Over voltage Protection	130% Vout for all outputs
Inrush Current	Less than 25A at 115 VAC
Transient response	Output voltage returns to within 1% in less than 500 μs on a 50 % Load Change. Peak transient not to exceed 5%
Holdup Time	30 watts minimum for 550mS after ACFAIL goes LOW. The supply is capable of holding up the Unit for two 500ms Power Loss periods occurring in a 1.5 second period.
Remote Sense	+5 VDC compensates 250 mV total line drop. Open sense load protection provided.
Fuse	Value: 2 Amps, Type: 3AG

5.3 2070-4A BLOCK DIAGRAM

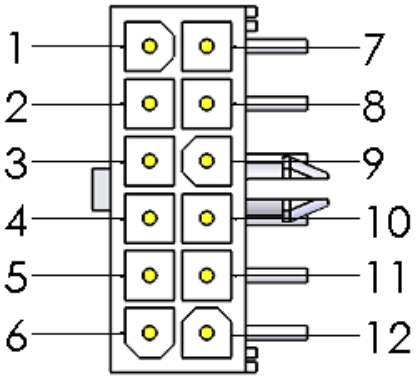


5.4 PS1 AND PS2 CONNECTORS' PIN OUT

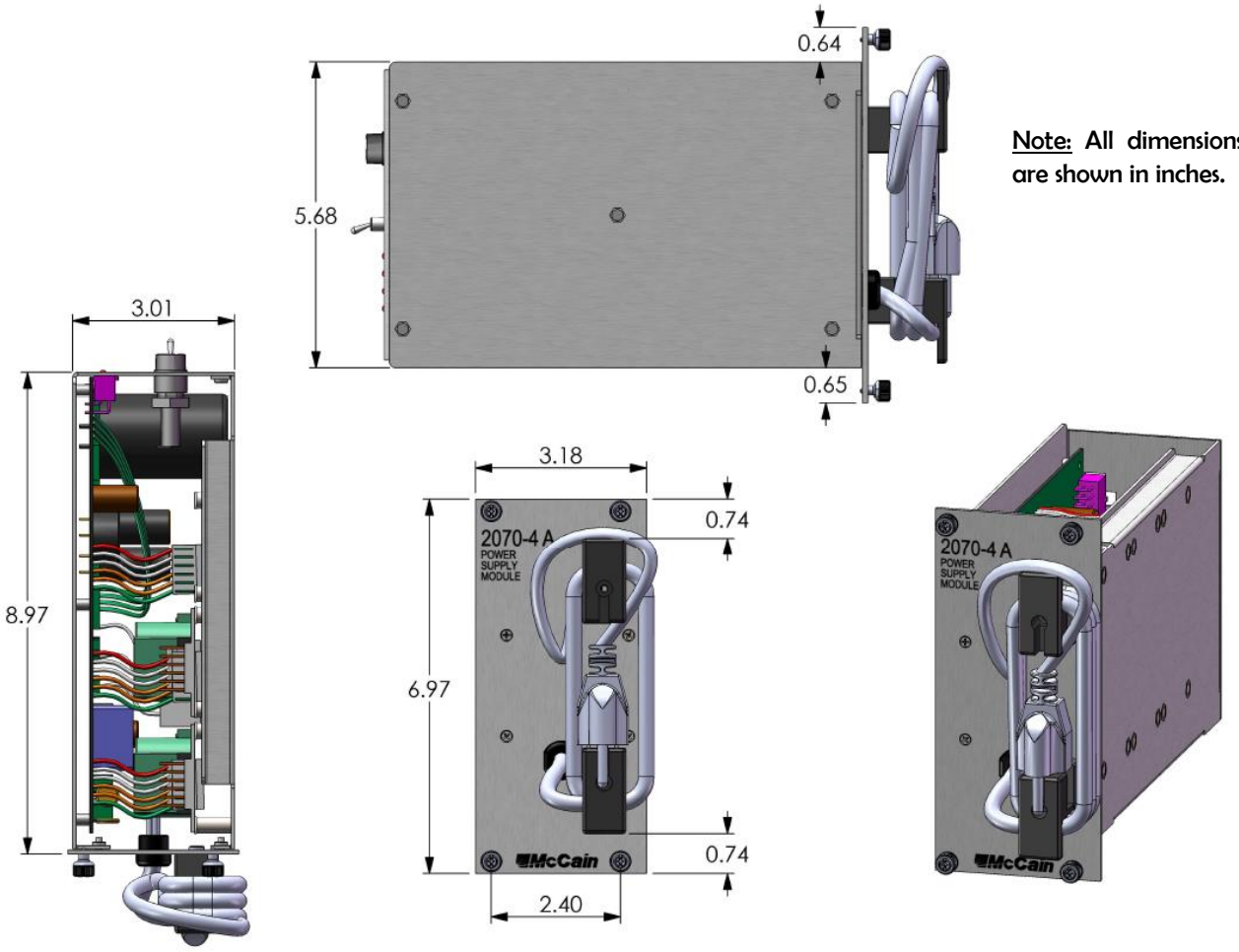
PS1 Connector	
Pin	Function
1	+5 VDC
2	+12 VDC SERIAL
3	-12 VDC SERIAL
4	DC GND #1 (+5 VDC & 12 SERIAL)
5	+5 VDC STANDBY
6	+5 VDC SENSE
7	DC GROUND SENSE
8	AC FAIL (VME)
9	SYSRESET (VME)
10	nc



PS2 Connector	
Pin	Function
1	+5 VDC
2	+12 VDC SERIAL
3	-12 VDC SERIAL
4	DC GND #1 (+5 VDC & 12 SERIAL)
5	+5 VDC STANDBY
6	+12 VDC ISO
7	DC GND (+12 VDC ONLY)
8	POWER DOWN / AC FAIL
9	POWER UP / SYS RESET
10	EQUIPMENT GROUND
11	LINESYNC
12	nc



5.5 2070-4A MODULE DIMENSIONS



Note: All dimensions are shown in inches.

Figure 10: 2070-4A Dimensions

5.6 ADJUSTMENT

There are four factory set adjustments of the Power Supply module and must not be moved.

One adjustment corresponds to the AC line voltage window:

- Power Fail: 92VAC ±2VAC.
- Power Recovery: 97VAC ±2VAC.

This is done via a potentiometer located at the edge of the Control board.

One adjustment is performed for each power module to be set at the DC voltage level required. This is done via a potentiometer located at each power module.

5.7 INSTALLING THE 2070-4A MODULE

Normally the controller has the 2070-4A module, but this section contains information of installation of the 2070-4A in case it is not.

1. Turn off the 2070-4A module before the installation. Turn the Power switch OFF.
2. Slide the module into its corresponding compartment from the back of the Chassis unit and attach it by tightening its four TSD #3 devices.
3. Plug the PS2 harness coming from the Serial motherboard.
4. Plug the AC cord into its corresponding AC outlet.
5. Turn the 2070-4A module on. Turn the Power switch ON.

These steps complete the 2070-4A installation into the Controller.

6 CHASSIS UNIT

6.1 GENERAL DESCRIPTION

The chassis unit is an aluminum enclosure that serves for containing and interconnecting the different 2070's modules depending on the selected configuration. It supports the installation of optional modules; for example, a power supply module, a front panel module, a CPU module, a Field I/O module, and two communications boards (modems, GPS, synchronous and/or asynchronous boards, etc); also blank filler plates can be installed for unused slots.

Chassis unit is designed to be convection cooled via vertical ventilation using slots in the top and bottom plates.

It can be shelf mounted or rack mounted with 170 CALTRANS facilities.

The chassis unit consists of:

- Top and bottom sides have slots for convection cooling and flushed nuts for accepting the thumbscrews of the modules to be installed; also they have flushed nut for installing the serial motherboard. Left side and right side have provisions for installing the hinge and latch and also for allowing the controller to be rack mounted.
- Screws are stainless steel, countersunk, Phillips, flat head, except for the ones for holding the serial mother board which are pan head.
- Serial motherboard with a wiring harness to be plugged to power supply PS2 receptacle connector and five DIN-96 receptacle connectors labeled as A1 to A5 for plugging optional modules.
- Card guides on top and bottom sides to allow modules slide and plug to the serial motherboard and also for installing the power supply module.
- The hinge on right side and latch on left side to hold and secure the front panel assembly.

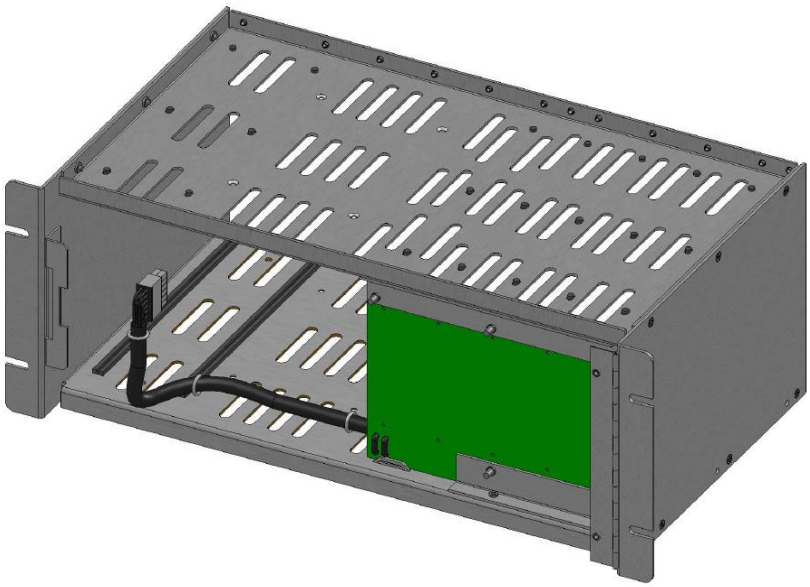
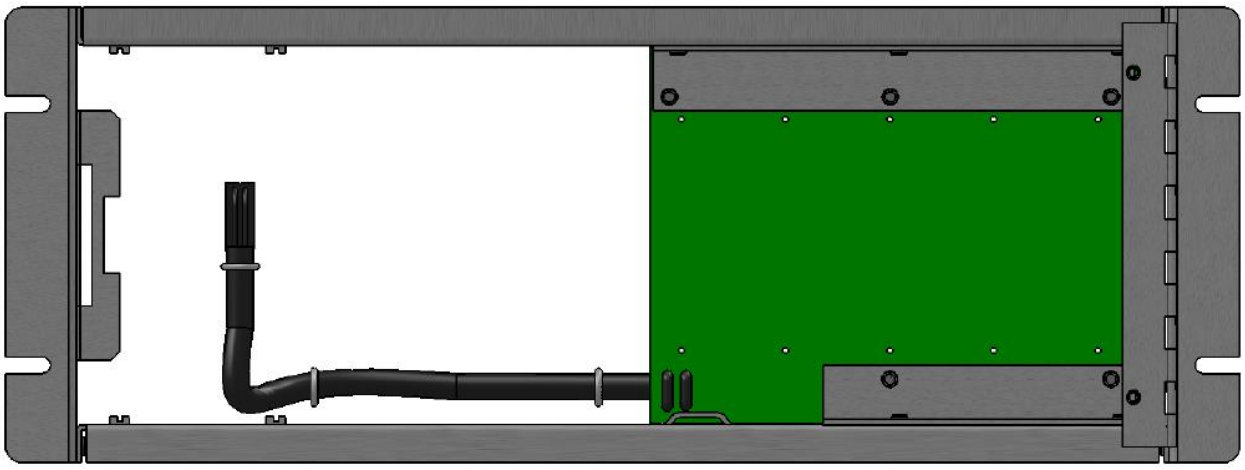
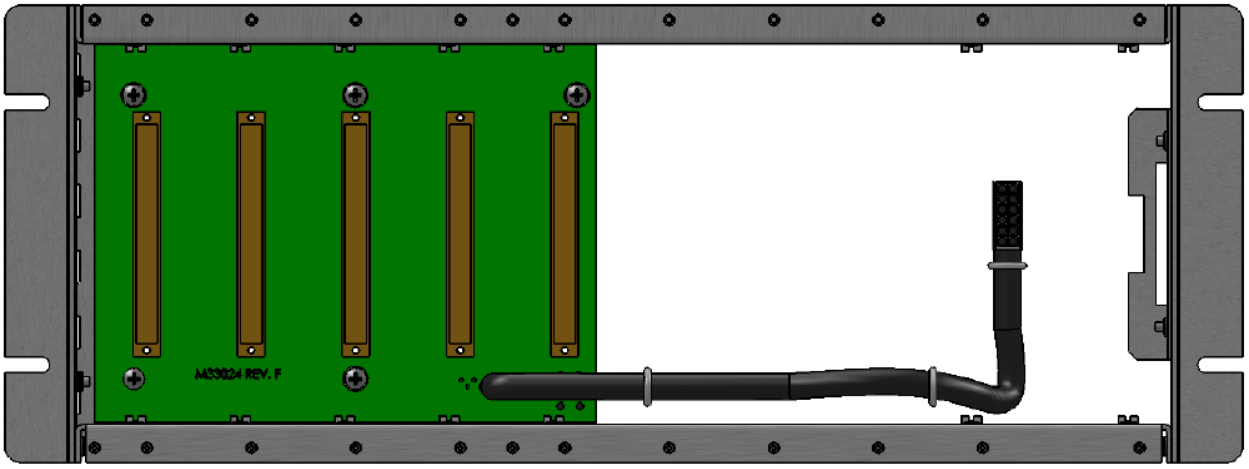


Figure 11: 2070LX Chassis unit



Chassis front view



Chassis rear view

Figure 12: Front and rear view 2070LX Chassis

6.2 SERIAL MOTHERBOARD

6.2.1 Theory of operation

The Serial Motherboard (Back plane) is a PCB sub-assembly that provides the interconnection of power lines and signals of the modules installed into the 2070 chassis. This means that it provides the buses for power, control and communication signals among the modules installed into slots A1 to A5, power supply and front panel.

The serial motherboard consists of:

- A multilayered PCB that provide the necessary interconnections among the connectors to be soldered to it.
- Five 96-positions DIN receptacle connectors labeled as A1 to A5 for plugging optional modules.
- A wiring harness to be plugged to power supply PS2 receptacle connector. It is soldered at PCB side, braided, tightened with wire ties and finished with crimped gold sockets loaded into a 12-positions plug connector.
- A 40-positions flat ribbon cable harness for connecting to the front panel module. It is soldered to the PCB side and finished with a 40-positions keyed plug receptacle.
- Support brackets with flushed nuts installed to be attached to the top and bottom sides of the chassis.
- Stainless steel, Phillips, pan head screws and washers; they are used to attach the brackets to the PCB and to the chassis.

The Motherboard receives power and control signals from the PS2 connector on power supply through the wiring harness soldered to the PCB; then Motherboard distributes the power and control signals to the five 96-pin DIN connectors and to the connector dedicated to the front panel interface. It also carries the serial communication among the dedicated modules and front panel module.

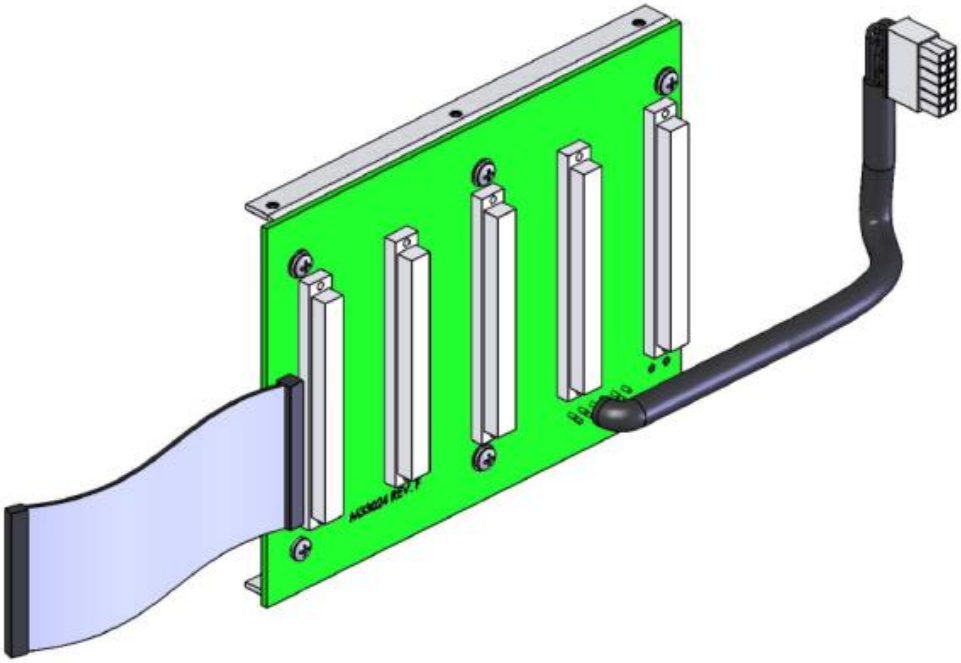
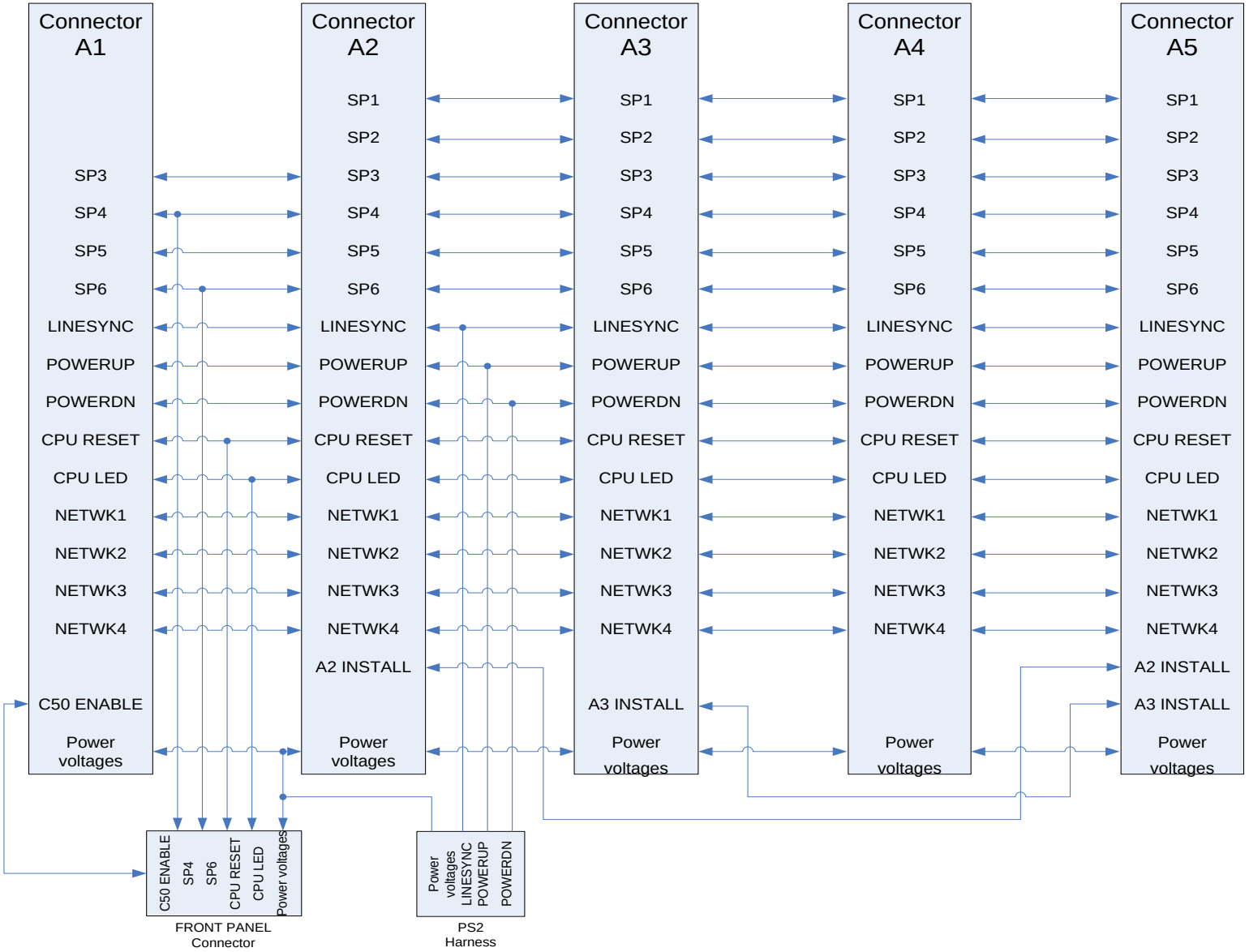


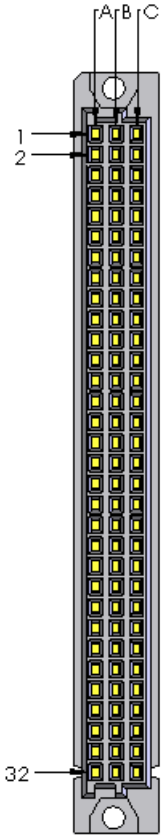
Figure 13: 2070 Serial motherboard

6.3 2070 SERIAL MOTHERBOARD BLOCK DIAGRAM

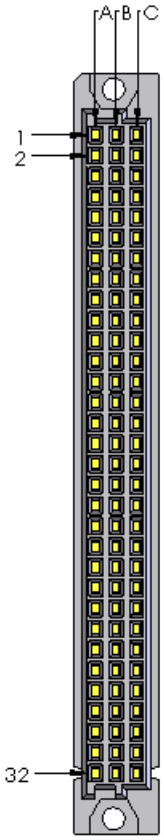


6.4 CONNECTORS' PIN OUT

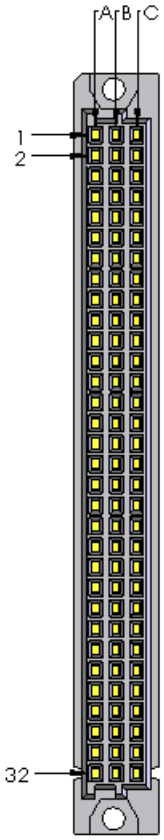
A1 Connector					
Pin	Function	Pin	Function	Pin	Function
A1	SP3TXD+	B1	SP6TXD+	C1	SP5TXD+
A2	SP3TKD-	B2	SP6TXD-	C2	SP5TXD-
A3	SP3RXD+	B3	SP6RXD+	C3	SP5TXC+
A4	SP3RXD-	B4	SP6RXD-	C4	SP5TXC-
A5	SP3RTS+	B5	SP3TXCO+	C5	SP5RXD+
A6	SP3RTS-	B6	SP3TXCO-	C6	SP5RXD-
A7	SP3CTS+	B7	SP3TXCI+	C7	SP5RXC+
A8	SP3CTS-	B8	SP3TXCI-	C8	SP5RXC-
A9	SP3DCD+	B9	SP3RXC+	C9	SP3TXD+
A10	SP3DCD-	B10	SP3RXC-	C10	SP3TXD-
A11	SP4TXD+	B11	SP4TXD+	C11	SP3RXD+
A12	SP4TXD-	B12	SP4TXD-	C12	SP3RXD-
A13	SP4RXD+	B13	SP4RXD+	C13	SP3RTS+
A14	SP4RXD-	B14	SP4RXD-	C14	SP3RTS-
A15	~	B15	~	C15	SP3CTS+
A16	~	B16	~	C16	SP3CTS-
A17	~	B17	~	C17	SP3DCD+
A18	~	B18	~	C18	SP3DCD-
A19	~	B19	~	C19	SP3TXCO+
A20	~	B20	~	C20	SP3TXCO-
A21	DCG#1	B21	C50ENABLE	C21	SP3TXCI+
A22	NETWK1	B22	~	C22	SP3RXCI-
A23	NETWK2	B23	~	C23	SP3RXC+
A24	~	B24	LINESYNC	C24	SP3RXC-
A25	NETWK3	B25	POWERUP	C25	CPURESET
A26	NETWK4	B26	POWERDOWN	C26	CPU LED
A27	DCG#1	B27	DCG#1	C27	DCG#1
A28	+12VDCSERIAL	B28	-12VDCSERIAL	C28	+5VDCSTANDBY
A29	5VDC	B29	+5VDC	C29	+5VDC
A30	DCG#1	B30	DCG#1	C30	DCG#1
A31	+12VDC	B31	+12VDC	C31	+12VDC
A32	DCG#2	B32	DCG#2	C32	DCG#2



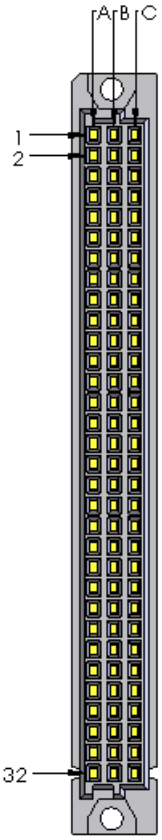
A2 Connector					
Pin	Function	Pin	Function	Pin	Function
A1	SP1TXD+	B1	SP6TXD+	C1	SP5TXD+
A2	SP1TKD-	B2	SP6TXD-	C2	SP5TXD-
A3	SP1RXD+	B3	SP6RXD+	C3	SP5TXC+
A4	SP1RXD-	B4	SP6RXD-	C4	SP5TXC-
A5	SP1RTS+	B5	SP1TXCO+	C5	SP5RXD+
A6	SP1RTS-	B6	SP1TXCO-	C6	SP5RXD-
A7	SP1CTS+	B7	SP1TXCI+	C7	SP5RXC+
A8	SP1CTS-	B8	SP1TXCI-	C8	SP5RXC-
A9	SP1DCD+	B9	SP1RXC+	C9	SP3TXD+
A10	SP1DCD-	B10	SP1RXC-	C10	SP3TXD-
A11	SP2TXD+	B11	SP4TXD+	C11	SP3RXD+
A12	SP2TXD-	B12	SP4TXD-	C12	SP3RXD-
A13	SP2RXD+	B13	SP4RXD+	C13	SP3RTS+
A14	SP2RXD-	B14	SP4RXD-	C14	SP3RTS-
A15	SP2RTS+	B15	SP2TXCO+	C15	SP3CTS+
A16	SP2RTS-	B16	SP2TXCO-	C16	SP3CTS-
A17	SP2CTS+	B17	SP2TXCI+	C17	SP3DCD+
A18	SP2CTS-	B18	SP2TXCI-	C18	SP3DCD-
A19	SP2DCD+	B19	SP2RXC+	C19	SP3TXCO+
A20	SP2DCD-	B20	SP2RXC-	C20	SP3TXCO-
A21	DCG#1	B21	~	C21	SP3TXCI+
A22	NETWK1	B22	~	C22	SP3RXCI-
A23	NETWK2	B23	A2INSTALLED	C23	SP3RXC+
A24	~	B24	LINESYNC	C24	SP3RXC-
A25	NETWK3	B25	POWERUP	C25	CPURESET
A26	NETWK4	B26	POWERDOWN	C26	CPU LED
A27	DCG#1	B27	DCG#1	C27	DCG#1
A28	+12VDCSERIAL	B28	-12VDCSERIAL	C28	+5VDCSTANDBY
A29	5VDC	B29	+5VDC	C29	+5VDC
A30	DCG#1	B30	DCG#1	C30	DCG#1
A31	+12VDC	B31	+12VDC	C31	+12VDC
A32	DCG#2	B32	DCG#2	C32	DCG#2



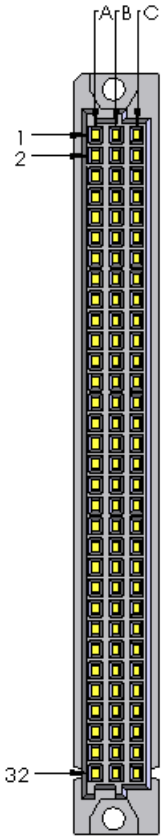
A3 Connector					
Pin	Function	Pin	Function	Pin	Function
A1	SP1TXD+	B1	SP6TXD+	C1	SP5TXD+
A2	SP1TKD-	B2	SP6TXD-	C2	SP5TXD-
A3	SP1RXD+	B3	SP6RXD+	C3	SP5TXC+
A4	SP1RXD-	B4	SP6RXD-	C4	SP5TXC-
A5	SP1RTS+	B5	SP1TXCO+	C5	SP5RXD+
A6	SP1RTS-	B6	SP1TXCO-	C6	SP5RXD-
A7	SP1CTS+	B7	SP1TXCI+	C7	SP5RXC+
A8	SP1CTS-	B8	SP1TXCI-	C8	SP5RXC-
A9	SP1DCD+	B9	SP1RXC+	C9	SP3TXD+
A10	SP1DCD-	B10	SP1RXC-	C10	SP3TXD-
A11	SP2TXD+	B11	SP4TXD+	C11	SP3RXD+
A12	SP2TXD-	B12	SP4TXD-	C12	SP3RXD-
A13	SP2RXD+	B13	SP4RXD+	C13	SP3RTS+
A14	SP2RXD-	B14	SP4RXD-	C14	SP3RTS-
A15	SP2RTS+	B15	SP2TXCO+	C15	SP3CTS+
A16	SP2RTS-	B16	SP2TXCO-	C16	SP3CTS-
A17	SP2CTS+	B17	SP2TXCI+	C17	SP3DCD+
A18	SP2CTS-	B18	SP2TXCI-	C18	SP3DCD-
A19	SP2DCD+	B19	SP2RXC+	C19	SP3TXCO+
A20	SP2DCD-	B20	SP2RXC-	C20	SP3TXCO-
A21	DCG#1	B21	~	C21	SP3TXCI+
A22	NETWK1	B22	~	C22	SP3RXCI-
A23	NETWK2	B23	A3INSTALLED	C23	SP3RXC+
A24	~	B24	LINESYNC	C24	SP3RXC-
A25	NETWK3	B25	POWERUP	C25	CPURESET
A26	NETWK4	B26	POWERDOWN	C26	CPU LED
A27	DCG#1	B27	DCG#1	C27	DCG#1
A28	+12VDCSERIAL	B28	-12VDCSERIAL	C28	+5VDCSTANDBY
A29	5VDC	B29	+5VDC	C29	+5VDC
A30	DCG#1	B30	DCG#1	C30	DCG#1
A31	+12VDC	B31	+12VDC	C31	+12VDC
A32	DCG#2	B32	DCG#2	C32	DCG#2



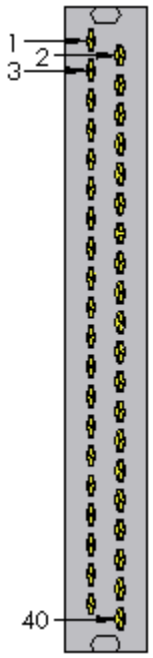
A4 Connector					
Pin	Function	Pin	Function	Pin	Function
A1	SP1TXD+	B1	SP6TXD+	C1	SP5TXD+
A2	SP1TKD-	B2	SP6TXD-	C2	SP5TXD-
A3	SP1RXD+	B3	SP6RXD+	C3	SP5TXC+
A4	SP1RXD-	B4	SP6RXD-	C4	SP5TXC-
A5	SP1RTS+	B5	SP1TXCO+	C5	SP5RXD+
A6	SP1RTS-	B6	SP1TXCO-	C6	SP5RXD-
A7	SP1CTS+	B7	SP1TXCI+	C7	SP5RXC+
A8	SP1CTS-	B8	SP1TXCI-	C8	SP5RXC-
A9	SP1DCD+	B9	SP1RXC+	C9	SP3TXD+
A10	SP1DCD-	B10	SP1RXC-	C10	SP3TXD-
A11	SP2TXD+	B11	SP4TXD+	C11	SP3RXD+
A12	SP2TXD-	B12	SP4TXD-	C12	SP3RXD-
A13	SP2RXD+	B13	SP4RXD+	C13	SP3RTS+
A14	SP2RXD-	B14	SP4RXD-	C14	SP3RTS-
A15	SP2RTS+	B15	SP2TXCO+	C15	SP3CTS+
A16	SP2RTS-	B16	SP2TXCO-	C16	SP3CTS-
A17	SP2CTS+	B17	SP2TXCI+	C17	SP3DCD+
A18	SP2CTS-	B18	SP2TXCI-	C18	SP3DCD-
A19	SP2DCD+	B19	SP2RXC+	C19	SP3TXCO+
A20	SP2DCD-	B20	SP2RXC-	C20	SP3TXCO-
A21	DCG#1	B21	~	C21	SP3TXCI+
A22	NETWK1	B22	~	C22	SP3RXCI-
A23	NETWK2	B23	~	C23	SP3RXC+
A24	~	B24	LINESYNC	C24	SP3RXC-
A25	NETWK3	B25	POWERUP	C25	CPURESET
A26	NETWK4	B26	POWERDOWN	C26	CPU LED
A27	DCG#1	B27	DCG#1	C27	DCG#1
A28	+12VDCSERIAL	B28	-12VDCSERIAL	C28	+5VDCSTANDBY
A29	5VDC	B29	+5VDC	C29	+5VDC
A30	DCG#1	B30	DCG#1	C30	DCG#1
A31	+12VDC	B31	+12VDC	C31	+12VDC
A32	DCG#2	B32	DCG#2	C32	DCG#2



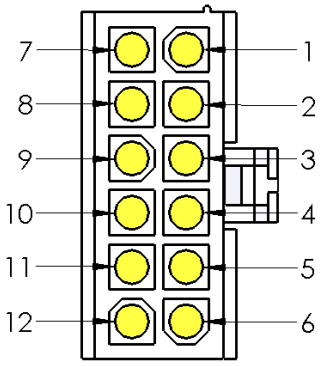
A5 Connector					
Pin	Function	Pin	Function	Pin	Function
A1	SP1TXD+	B1	SP6TXD+	C1	SP5TXD+
A2	SP1TKD-	B2	SP6TXD-	C2	SP5TXD-
A3	SP1RXD+	B3	SP6RXD+	C3	SP5TXC+
A4	SP1RXD-	B4	SP6RXD-	C4	SP5TXC-
A5	SP1RTS+	B5	SP1TXCO+	C5	SP5RXD+
A6	SP1RTS-	B6	SP1TXCO-	C6	SP5RXD-
A7	SP1CTS+	B7	SP1TXCI+	C7	SP5RXC+
A8	SP1CTS-	B8	SP1TXCI-	C8	SP5RXC-
A9	SP1DCD+	B9	SP1RXC+	C9	SP3TXD+
A10	SP1DCD-	B10	SP1RXC-	C10	SP3TXD-
A11	SP2TXD+	B11	SP4TXD+	C11	SP3RXD+
A12	SP2TXD-	B12	SP4TXD-	C12	SP3RXD-
A13	SP2RXD+	B13	SP4RXD+	C13	SP3RTS+
A14	SP2RXD-	B14	SP4RXD-	C14	SP3RTS-
A15	SP2RTS+	B15	SP2TXCO+	C15	SP3CTS+
A16	SP2RTS-	B16	SP2TXCO-	C16	SP3CTS-
A17	SP2CTS+	B17	SP2TXCI+	C17	SP3DCD+
A18	SP2CTS-	B18	SP2TXCI-	C18	SP3DCD-
A19	SP2DCD+	B19	SP2RXC+	C19	SP3TXCO+
A20	SP2DCD-	B20	SP2RXC-	C20	SP3TXCO-
A21	DCG#1	B21	A2INSTALLED	C21	SP3TXCI+
A22	NETWK1	B22	DCG#1	C22	SP3RXCI-
A23	NETWK2	B23	A3INSTALLED	C23	SP3RXC+
A24	~	B24	LINESYNC	C24	SP3RXC-
A25	NETWK3	B25	POWERUP	C25	CPURESET
A26	NETWK4	B26	POWERDOWN	C26	CPU LED
A27	DCG#1	B27	DCG#1	C27	DCG#1
A28	+12VDCSERIAL	B28	-12VDCSERIAL	C28	+5VDCSTANDBY
A29	5VDC	B29	+5VDC	C29	+5VDC
A30	DCG#1	B30	DCG#1	C30	DCG#1
A31	+12VDC	B31	+12VDC	C31	+12VDC
A32	DCG#2	B32	DCG#2	C32	DCG#2



Front Panel Connector			
Pin	Function	Pin	Function
1	SP4TXD+	2	SP4TXD-
3	SP4RXD+	4	SP4RXD-
5	SP6TXD+	6	SP6TXD-
7	SP6RXD+	8	SP6RXD-
9	~	10	~
11	~	12	~
13	~	14	~
15	~	16	~
17	~	18	~
19	~	20	~
21	DCG#1	22	DCG#1
23	+12VDCSERIAL	24	-12VDCSERIAL
25	DCG#1	26	DCG#1
27	CPU LED	28	DCG#1
29	CPURESET	30	DCG#1
31	DCG#1	32	C50ENABLE
33	DCG#1	34	+5VDC
35	+5VDC	36	+5VDC
37	+5VDC	38	+5VDC
39	~	40	~



PS2 Connector			
Pin	Function	Pin	Function
1	+5VDC	7	DCG#2
2	+12VDCSERIAL	8	POWERDOWN
3	-12VDCSERIAL	9	POWERUP
4	DCG#1	10	EQUIPMENT GROUND
5	+5VDCSTANDBY	11	LINESYNC
6	+12VDC	12	DCG#1



7 GENERAL SPECIFICATIONS

Style: Caltrans 2070

Dimensions: 7” H x 19” W x 13” D (rounded to the nearest inch)

Form factor: Shelf mount or 19” EIA (Electronics Industry Alliance) rack mount

Weight: ± 12.5 lbs (based on final module selection)

Power:

AC voltage: 85 VAC to 135 VAC

Frequency: 60 Hz (± 3 Hz)

Power supply output specifications:

+5.0 VDC: 1.0 A - 10.0 A

+12.0 VDC Serial: 0.1 A - 0.5 A

–12.0 VDC Serial: 0.1 A - 0.5 A

+12.0 VDC ISO: 0.1 A - 1.0 A

Environment:

Operating Temperature: -37° C to +74° C

Humidity: 0 to 95% (non-condensing)